The Transistor - Source Companion

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Citation tags in the text - [H#] history, [T#] technology, [I#] industry, [M#] markets/process, [P#] physics/policy, [L#] lithography, [G#] industry structure, [N#] devices/applications, [B#] business/power, [F#] future devices, [E#] energy, [S#] late-2026 status checks - resolve here. Each entry records what the source supports, its limits, and how deeply it was read (FULL / EXCERPT / ABSTRACT / SEARCH-RESULT).

H1 - Computer History Museum, “1947: Invention of the Point-Contact Transistor” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: Shockley returned early 1945 to organize solid-state group under Mervin Kelly’s encouragement; April 1945 field-effect amplifier concept failed; Bardeen’s surface-states explanation; Dec 16, 1947 first successful semiconductor amplifier (point-contact, germanium, two gold contacts, plastic wedge); voltage on one contact modulated current through the other, amplification up to 100x; Dec 23, 1947 demonstration to lab officials (“magnificent Christmas present” per Shockley); named “transistor” by John Pierce; announced at NYC press conference June 30, 1948; Type A production model in metal cartridge, many thousands produced despite delicate construction. URL: https://www.computerhistory.org/siliconengine/invention-of-the-point-contact-transistor/

M1 - Semiconductor Industry Association, “Global Annual Semiconductor Sales Increase 25.6% to $791.7 Billion in 2025” (Feb 6, 2026)

Read: FULL (web page, 2026-11-01) Supports: 2025 global semiconductor sales $791.7B, +25.6% vs 2024’s $630.5B; Q4 2025 $236.6B (+37.1% YoY); Dec 2025 $78.9B; SIA projection ~$1T for 2026 (Neuffer quote); logic largest category $301.9B (+39.9%); memory second $223.1B (+34.8%); regional: Asia Pacific/All Others +45.0%, Americas +30.5%, China +17.3%, Europe +6.3%, Japan -4.7%; WSTS compiles monthly as 3-month moving average; SIA represents 99% of US industry by revenue, ~2/3 of non-US firms. URL: https://www.semiconductors.org/global-annual-semiconductor-sales-increase-25-6-to-791-7-billion-in-2025/

I1 - Tom’s Hardware (Anton Shilov), “TSMC begins quietly volume production of 2nm-class chips” (Dec 29, 2025)

Read: FULL (web page, 2026-11-01) Supports: TSMC N2 volume production commenced 4Q25 as planned, no formal press release; first TSMC GAA nanosheet node; vs N3E: +10-15% performance at same power, -25-30% power at same performance, +15% density (mixed), up to +20% logic-only; N2P and A16 (Super Power Rail backside delivery) HVM H2 2026; N2X 2027; production at Fab 22 near Kaohsiung (Fab 20 Hsinchu later); C.C. Wei October earnings call quote “N2 is well on track for volume production later this quarter, with good yield... faster ramp in 2026, fueled by both smartphone and HPC AI applications”; simultaneous ramp of smartphone and HPC/AI designs unusual. Limitations: trade press; company data compiled from calls/briefings. URL: https://www.tomshardware.com/tech-industry/semiconductors/tsmc-begins-quietly-volume-production-of-2nm-class-chips-first-gaa-transistor-for-tsmc-claims-up-to-15-percent-improvement-at-iso-power

I2 - TSMC, “2nm Technology” (company technology page)

Read: FULL (web page, 2026-11-01) Supports: TSMC's own statement "TSMC's 2nm (N2) technology has started volume production in 4Q25 as planned." Company self-description as provider of advanced dedicated foundry process technologies. Limitations: vendor page; proves company's own claims/offerings only. URL: https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_2nm

H2 - Computer History Museum, "Timeline" (The Silicon Engine)

Read: FULL (timeline page, 2026-11-01; 68 dated entries) Supports: the milestone spine 1833-1970s+: 1833 Faraday silver sulfide conduction vs temperature; 1874 Braun point-contact rectification on galena; 1901 Bose cat's-whisker patent; 1926 Lilienfeld field-effect patent; 1931 Wilson quantum theory of semiconductors, 1938 Davydov/Mott/Schottky rectification theory; 1940 Ohl p-n junction + photovoltaic; 1941 WWII high-purity Ge/Si for radar detectors; 1947 point-contact; 1948 Mataré & Welker independent French point-contact; 1948 Shockley junction conception; 1951 Pfann & Theurer zone refining; 1951 Teal grows large single-crystal Ge, with Sparks n-p-n grown junction; 1952 hearing aids/pocket radios; 1952 Bell symposia + licensing; 1953 transistorized computer prototype; 1954 Lee & Tanenbaum diffusion process; 1954 Tanenbaum first silicon transistor at Bell, TI first commercial silicon devices; 1955 Andrus & Bond photolithography from printing; 1955 Frosch & Derick oxide masking; 1956 Shockley Semiconductor in NorCal; 1958 Kilby solid circuit; 1958 Fairchild double-diffused silicon mesa production; 1958 Esaki tunnel diode (Sony); 1959 Noyce monolithic IC patent on Hoerni planar; 1959 Hoerni planar process for mesa reliability; 1960 epitaxy; 1960 Atalla & Kahng MOS demonstration; 1960 Last first planar IC; 1961 test equipment market; 1961 Cray-funded silicon speed record; 1962 aerospace first IC computer use; 1963 DTL families, TTL dominant by late 1960s; 1963 Wanlass CMOS; 1964 General Microelectronics first commercial MOS IC (calculator); 1964 Talbert & Widlar analog ICs; 1964 IBM S/360 SLT hybrid; 1965 ROM chips, DIP package, mainframe ICs, Moore's law prediction; 1966 IBM CAD tools, bipolar RAMs, ASICs; 1967 turnkey equipment vendors; 1968 Faggin & Klein silicon gate, Fairchild 3708 first commercial silicon-gate IC; Schottky TTL; 1970s: Intel 1103 DRAM vs core, microprocessor, Frohman(-Bentchkowsky) EPROM, Dennard scaling paper, TMS1000 MCU, Microma watch first SoC. Limitations: curated timeline entries (terse); dates/attributions need chapter-level corroboration for strong claims. URL: https://www.computerhistory.org/siliconengine/timeline/

H3 - Computer History Museum, "1948: Conception of the Junction Transistor" (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: After Dec 1947, Shockley's month of intense theory; Jan 23, 1948 conceived junction transistor based on Ohl's 1940 p-n junction; partly spurred by professional jealousy at exclusion from point-contact work; recognized point-contact's delicate construction would be hard to manufacture reliably; disagreed with Bardeen's surface explanation - claimed holes penetrate bulk germanium ("minority carrier injection"), crucial to junction transistor; three-layer n-p-n sandwich; Feb 16, 1948 John Shive demonstrated transistor action with point contacts on opposite sides of a germanium sliver, proving holes flow through bulk; patent filed June 1948 (US 2,569,347, issued Sept 25, 1951); theory published July 1949 BSTJ; 1950 book Electrons and Holes in Semiconductors; two more years to manufacture in quantity (1951). Primary refs listed: Shockley lab notebook 20455 pp128-32; 1976 IEEE TED retrospective; Riordan & Hoddeson Crystal Fire pp142-55. URL: https://www.computerhistory.org/siliconengine/conception-of-the-junction-transistor/

H4 / M6 - Computer History Museum, "1959: Invention of the 'Planar' Manufacturing Process" (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: Hoerni's Dec 1957 recorded idea: leave oxide layer in place to protect p-n junctions; Fairchild too busy getting first devices into production to pursue; conventional wisdom required removing oxide after masking; Jan 1959 patent disclosure; March 1959 working planar transistor demonstrated; oxide protected junctions as predicted; better electrical characteristics, far lower leakage (critical for computer logic); enabled fabrication of all IC components from one side of wafer; 2N1613 planar transistor commercial April 1960; licensed across the industry; billion-transistor ICs rely on it; "One historian has called it 'the most important innovation in the history of the semiconductor industry'" (CHM's phrasing, unattributed there); 1960s failure mechanisms: purple plague on gold bond wires, electromigration of aluminum interconnect, MOS stability. Patent US 3,025,589 filed May 1, 1959, issued March 20, 1962. URL: https://www.computerhistory.org/siliconengine/invention-of-the-planar-manufacturing-process/ Note: registered twice under [H4] and [M6] (device-history and manufacturing tracks); merged into this single entry. [M6] citations in the text resolve here.

H5 - APS News (Kendra Redmond), "Nov. 16, 1904: John Ambrose Fleming Patents the Vacuum Tube" (Oct 15, 2024)

Read: FULL (web page, 2026-11-01) Supports: Edison effect: charge flows from glowing filament to metal probe only when probe positive (Edison's 1880s lamp experiments, patented lamp-style voltage indicator); Fleming studied under Maxwell at Cambridge/Cavendish; scientific advisor to Edison Electric Light Co. London branch, later to Marconi's Wireless Telegraphy Co.; 1901 first transatlantic wireless exposed detection/amplification problems; coherer "exasperating" (MacGregor-Morris quote); October 1904 insight: open metal cylinder around filament = rectifier for radio detection; patent application one month later (Nov 16, 1904); de Forest's similar 1905 device; Fleming's US patent eventually ruled invalid; later modifications made tubes detectors, amplifiers, oscillators for radio, telephones, television; Dylla & Corneliussen (2005, JVST A): "Fleming's vacuum tube inaugurated the age of electronics - and dominated it until the advent of the transistor"; Fleming knighted 1929, died 1945 as Television Society of London president. URL: https://www.aps.org/apsnews/2024/10/ambrose-fleming-patents-vacuum-tube

H6 - NobelPrize.org, "The Nobel Prize in Physics 1956" (summary page)

Read: FULL (web page, 2026-11-01) Supports: 1956 Nobel Prize in Physics awarded jointly to Shockley, Bardeen, Brattain, 1/3 share each, "for their researches on semiconductors and their discovery of the transistor effect." URL: https://www.nobelprize.org/prizes/physics/1956/summary

H7 - NobelPrize.org, Presentation Speech by Prof. E.G. Rudberg (1956 ceremony)

Read: FULL (web page, 2026-11-01) Supports: period framing and readable physics: conductors ~1 carrier per atom vs insulators almost none; semiconductors in between; “artificial products made from elements such as germanium or silicon”; phosphorus donates electron to silicon; boron steals electron leaving mobile positive hole; “A few parts in 100,000 make a good semiconductor”; two-carrier idea from 1930s; failed pre-war attempts to control rectifiers with extra electrode like a valve grid; 1948 discovery of transistor action as the key to the control mechanism; rectification and hole-injection explanation of transistor action; transistor “functions much like a radio valve. But it is smaller, and it does not require current to heat a filament. Hearing aids, computing machines, telephone stations and many others are in need of just such a device”; Bardeen/Brattain probe mapping under microscope with micrometer screw; Murray Hill location; Franklin-to-Murray-Hill closing. Limitations: 1956 period piece; not a current source. URL: https://www.nobelprize.org/prizes/physics/1956/ceremony-speech/

H8 - Computer History Museum, “1940: Discovery of the p-n Junction” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: mid-1930s Ohl (electrochemist, Bell Labs Holmdel NJ) investigating silicon rectifiers as radar detectors; purity improved detection; 23 February 1940 slab test - current jumped under bright light; different crystal regions opposite effects with cat’s-whisker probe; with Jack Scaff found seam separating regions of distinct impurities: phosphorus excess electrons (n-type), boron deficiency/holes (p-type); the “p-n junction” barrier; photovoltaic effect; patent filed May 27, 1941 (US 2,402,662); Scaff & Ohl BSTJ 1947 paper on silicon radar rectifiers; Shockley’s 1948 junction conception derived from Ohl’s discovery. URL: https://www.computerhistory.org/siliconengine/discovery-of-the-p-n-junction/

H9 - Computer History Museum, “1951: First Grown-Junction Transistors Fabricated” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: fabrication blocked on pure uniform material; Teal argued for large single crystals, few listened incl. Shockley; built crystal-growing equipment with John Little and Ernest Buehler; based on Czochralski 1917 method - seed crystal withdrawn slowly from melt; Shockley later called it “the most important scientific development in the semiconductor field in the early days”; Sparks dropped impurity pellets into melt during growth; April 1950 two-pellet n-p-n with thin base layer; a year later grown-junction surpassed best point-contact; announced July 4, 1951 press conference with Shockley; patents Teal US 2,727,840 (filed June 15, 1950), Sparks & Teal US 2,631,356; Physical Review July 1951 paper (Shockley, Sparks, Teal). URL: https://www.computerhistory.org/siliconengine/first-grown-junction-transistors-fabricated/

H10 - Computer History Museum blog (David A. Laws, Semiconductor Curator), “13 Sextillion & Counting” (April 2, 2018)

Read: FULL (web page, 2026-11-01) Supports: MOS transistor called “the most frequently manufactured human artifact in history” (historian David C. Brock’s assessment, CHM CORE 2015); Jim Handy estimates: 2.9 sextillion transistors manufactured by 2014, updated to 13 sextillion (as of ~2018), total “increases by multiple billions every day”; 99.9% of shipped transistors are MOS; MOS sandwich structure explanation; acronym soup IGFET/MESFET/MISFET/MOSFET/MOST; Lilienfeld patents 1925-1928 (Canada+US), no evidence he built working units, Bardeen’s 1988 acknowledgment he “had the basic concept of controlling the flow of current in a semiconductor”; late 1930s Bell Labs charged Shockley with solid-state replacement for triode; RCA’s William Webster directed duplication; Tom Stanley quote: MOS seen “as an interesting niche device... slow and would never be a threat to bipolar transistors”; Stanley to Hofstein: “career killer... you have no career to kill”; Hofstein & Heiman 1961 first MOS IC arrays using Hoerni planar; Wanlass 1963: CMOS patent (zero power when not in use) + floating gate as memory element; GMe first commercial MOS IC 1964 (20-bit shift register; Victor Comptometer calculator chipset); calculator project failure doomed GMe, delayed MOS; Moore quote: “It was easy to make a device that worked, but we could not make one whose characteristics were stable... something was happening at the silicon-oxide interface that we did not understand”; Deal/Grove/Snow experiments 1963-66; “Fairchild never was a major participant in the market for MOS devices... the main cause of this was Fairchild’s great success in bipolar circuits”; Balk at IBM Yorktown, Kooi at Philips; early 1970s MOS mainstream → memories, microprocessors; enabled Intel, Micron formation. URL: https://computerhistory.org/blog/13-sextillion-counting-the-long-winding-road-to-the-most-frequently-manufactured-human-artifact-in-history/

I3 - NVIDIA, “Blackwell Architecture” (product page)

Read: FULL (web page, 2026-11-01) Supports: company claims: Blackwell-architecture GPUs pack 208 billion transistors; manufactured on custom TSMC 4NP process; two reticle-limited dies connected by 10 TB/s chip-to-chip interconnect as unified GPU; GB300 NVL72 delivers 65x Hopper AI compute; NVLink scales to 576 GPUs. Limitations: vendor marketing page; specifications are company claims, dated by access (2026-11-01). URL: https://www.nvidia.com/en-us/data-center/technologies/blackwell-architecture/

H11 - Computer History Museum, “ENIAC” (Revolution exhibit)

Read: FULL (web page, 2026-11-01) Supports: Mauchly 1942 proposal for all-electronic calculator; Army ballistics-tables need; built 1943-1945 at Moore School; “first large-scale computer to run at electronic speed without being slowed by any mechanical parts” (CHM’s description); programmers Frances Bilas and Betty Jean Jennings; ~18,000 vacuum tubes; lost one tube roughly every day or two; maintenance team got repairs down to about 15 minutes; strict design guidelines, tubes run well below maximum voltages for life; declassified after WWII; ended by a 1955 lightning strike. URL: https://www.computerhistory.org/revolution/story/78

H12 - IEEE Reach, “Lee de Forest - Audion” (primary sources)

Read: FULL (web page, 2026-11-01) Supports: 25 October 1906 de Forest patent application “Device for amplifying feeble electrical currents” including first form of 3-electrode Audion; became standard for inexpensive amplification of wireless voice signals and electronic instruments; in widespread use until replaced by the transistor. URL: https://reach.ieee.org/primary-sources/lee-de-forest-audion/

H13 - Patrick Mitchell (Electronics World, Aug 2000), “A History of the Grid” (r-type.org)

Read: FULL (web page, 2026-11-01) Supports: origin traced to Edison’s 1883 ’electrical indicator’ patent - one-way current filament to electrode, unused; Fleming advisor to Edison Electric Light Co. London 1882; bulb blackening research; 1899 advisor to Marconi; detector the weakest link; 1904 ’oscillation valve’ patents; de Forest Yale PhD 1899; McCandless lamp firm copies; October 1906 first three-electrode Audion patent (parallel plates, amplification doubtful); grid-iron bent wire third electrode between filament and anode; bulbs delivered 25 November 1906; tested 31 December 1906 - definite amplification; patent 29 January 1907; European cathode-ray amplifier work preceded; early triodes temperamental, varied, short-lived; pre-WWI patent litigation stagnated the art; patents suspended for WWI military work; Langmuir at GE from 1909 - gain via grid closer to cathode, thoriated tungsten cathode; 1915 Langmuir (GE) and Schottky (Siemens) simultaneously add screen grid = tetrode; Miller capacitance, secondary emission, microphony problems; vari-mu valves mid-1920s; WE 417A grid wires 7.4 microns. Limitations: technical enthusiast site reprinting a magazine article; detailed but secondary. URL: https://r-type.org/articles/art-222.htm

H14 - Paul Hart, “History of Vacuum Tube Manufacturing in the US From WWII to the End” (Radio Activity/MAARC presentation, June 3, 2022)

Read: FULL (PDF slides, 2026-11-01) Supports: US tube production 1945 = 139 million vs 108 million in 1940; Western Electric 1944: 1,540,000 tubes produced, 1,543,000 subcontracted, services ordered 3,395,000 from others to WE designs (e.g. 6AK5); WE 1974: 1.2M tubes; WE Kansas City plant closed 1988, last tube the 300B audio triode; by 1966 four majors remained: RCA 34%, GE 30%, GTE/Sylvania 30%, Westinghouse 6%; “by 1966 solid state had not been commercialized as fast as many experts had expected”; 1967 majority of radios/phonographs converted to solid state; 1974 microprocessor introduced, last hybrid TV sold; 1978 Zenith Trans-Oceanic 7000 last American-made radio; AT&T 1984 perspective quoted: “The transistor was not an accident: AT&T had determined prewar that the evolving telephone system would be untenable with vacuum tubes”; RCA patent pool 1920 (GE/AT&T cross-license, 7.5% royalty), Zenith litigation, RCA 1958 no-contest antitrust plea. Limitations: enthusiast presentation with an editorial agenda (US consumer-electronics decline); internal conflict: a slide headlined “1955 The Highest Production Year” but a later chart note reads “(Note 1966 peak)” - peak year unresolved in this source; production numbers attributed in-deck to “Declining Demand, Harrigan, pgs 77-78”. URL: https://maarc.org/wp-content/uploads/simple-file-list/Monthly_Mtg_Presentations/History_of_Tube_Manufacturing_in_the_US-053022.pdf

H15 - Computer History Museum, “1941: Semiconductor diode rectifiers serve in WW II” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: radar receivers needed solid-state rectifiers for microwave signals beyond vacuum-tube diodes; Si and Ge emerged dominant via wartime R&D; under MIT Radiation Laboratory, silicon purification mainly at U. Penn (Frederick Seitz) and DuPont; silicon of 99.999% purity by war’s end; germanium research at Purdue under Lark-Horovitz; “In 1947 Walter Brattain used a slab of the high-purity germanium developed at Purdue in fabricating the first, point-contact transistor”; Bell’s Scaff and Theurer mapped impurities to n-type (column V e.g. phosphorus) and p-type (column III e.g. boron); millions of crystal rectifier diodes fabricated for Allied radar receivers; key refs: Scaff & Ohl BSTJ Jan 1947; Torrey & Whitmer Crystal Rectifiers (MIT Rad Lab Series vol 15, 1948). URL: https://www.computerhistory.org/siliconengine/semiconductor-diode-rectifiers-serve-in-ww-ii/

H16 - Ralph Bray, “The Origin of Semiconductor Research at Purdue” (Purdue Physics memoir)

Read: FULL (web page, 2026-11-01) Supports: March 1942 OSRD/NDRC grant for improved point-contact crystal rectifier; wartime revival of crystal rectifiers because low capacitance suited microwave frequencies; English “red-dot” silicon detectors in 1942; germanium chosen over silicon/galena for lower melting point and crucible tolerance; graduate student Randy Whaley assigned crystal growing + Eagle-Picher contact (Ge byproduct of tin production); purification: GeO2 reduced in hydrogen, prolonged vacuum heating; Benzer’s high back-voltage (>100V) germanium rectifier solved electrical burnout, patented by Purdue with royalties split, mass-produced at Bell Labs; Seitz’s Modern Theory of Solids (1940) never mentioned silicon or germanium; by war’s end: column III dopants -> p-type, column V -> n-type; n-type gave good rectifiers, p-type did not (unexplained); “a germanium crystal made at Purdue eventually was used for the first transistor built at Bell Laboratories”; KLH’s leadership, nightly lab lights, secrecy. Limitations: personal memoir (written decades later); Lark-Horovitz’s reluctance to publish meant credit disputes (“appropriate credit failed to accrue”). URL: https://www.physics.purdue.edu/about/history/semi_conductor_research.html

H17 - PBS “Transistorized!”, “Solid State Science Takes Root at Bell”

Read: FULL (web page, 2026-11-01) Supports: August 1945 Bell Labs reorganization driven by Kelly; Solid State Physics group created; Shockley and chemist Stanley Morgan in charge; Brattain, Gerald Pearson, Robert Gibney transferred in; Bardeen hired; Shockley ran semiconductor subdivision; quantum theory base from Wigner/Seitz 1930s; group culture quotes (Brattain: “I cannot overemphasize the rapport of this group...”; Joel Shurkin: “Shockley had enough brains to leave them alone...”); military as likely customer with lavish Cold War funding. URL: https://www.pbs.org/transistor/background1/events/ssgroup.html

H18 - PBS “Transistorized!”, “Sharing the Technology: Bell Hosts Transistor Symposia”

Read: FULL (web page, 2026-11-01) Supports: September 1951 first symposium, ~300 scientists and engineers; licensing fee $25,000; 26 companies US and abroad signed (IBM, GE among big; Texas Instruments among small); April 1952 Transistor Technology Symposium, over 100 registrants, eight days of day-and-night work; proceedings bound as two-volume “Transistor Technology” = “Mother Bell’s Cookbook”; Jack Morton quote (Electronics, 19 Feb 1968): “We realized that if this thing was as big as we thought, we couldn’t keep it to ourselves and we couldn’t make all the technical contributions. It was in our interest to spread it around. If you cast your bread on the water, sometimes it comes back angel food cake.” Limitations: says eight days; CHM [H19] says nine-day - duration conflict noted, duration avoided in prose. URL: https://www.pbs.org/transistor/background1/events/symposia.html

H19 - Computer History Museum, “1952: Bell Labs Licenses Transistor Technology” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: Jack Morton led “fundamental development” program; Morton advocated sharing because AT&T could benefit from advances elsewhere; three gatherings during the 1950s; September 1951 first meeting specifically addressed military users/applications; April 1952: over 100 representatives from 40 companies that had paid a $25,000 patent-licensing fee; visit to Western Electric’s Allentown PA transistor plant; participants from GE, RCA, plus then-small Texas Instruments and Sony; “Ma Bell’s Cookbook” = Transistor Technology vols I-III (Van Nostrand 1958) “became the bible of the dynamic semiconductor industry that emerged in the 1950s.” URL: https://www.computerhistory.org/siliconengine/bell-labs-licenses-transistor-technology/

H20 - PBS “Transistorized!”, “Mervin Kelly” (bio)

Read: FULL (web page, 2026-11-01) Supports: Kelly as research director drove Bell into solid state; background in vacuum tubes; late 1930s, after hundreds of thousands of dollars spent improving tubes without progress, changed his mind; promoted to research director 1936; hired young PhDs incl. Shockley; post-war reorganization formed solid state department; invested heavily to make the transistor workable; failed to resolve Bardeen-Shockley friction and lost Bardeen to University of Illinois; Bell president 1951-1959; transistors became standard in phone service during his tenure; laser and solar cell also developed at Bell under him; Walter Brown’s sleeping-Kelly anecdote. URL: https://www.pbs.org/transistor/album1/addlbios/kelly.html

H21 - CHM blog (David A. Laws), “’The Surface State Job’” (Dec 12, 2022)

Read: FULL (web page, 2026-11-01) Supports: project code name “The Surface State Job”; Brattain carpool quote; biographies (Brattain b. Amoy China 1902, ranch near Tonasket WA, Oregon MSc, Minnesota PhD, joined Bell 1929; Bardeen b. Madison 1908, child prodigy, Wisconsin MSc, Princeton PhD); Kelly recruited Shockley from MIT in 1936; Shockley b. London to American parents, raised in Palo Alto yards from the HP garage, Caltech BS, MIT PhD; Moore: Shockley “could see electrons”; Townes: “He understood everything but people”; Shockley’s 1939 notebook: “It has today occurred to me that an amplifier using semiconductors rather than vacuum is in principle possible”; March 19, 1946 Bardeen’s trapped-electron surface-state theory; early 1947 experimental confirmation; Gibney’s Nov 17 suggestion (metal plate + electrolyte); Nov 21 Brattain’s low-frequency amplifier; Magic Month; Bardeen’s two-close-contacts calculation; Brattain’s gold-foil plastic wedge sliced with razor (contacts a sheet of paper’s width apart); afternoon of Tuesday December 16, 1947 - spring-loaded wedge on germanium, “amplifier with the order of magnitude of 100 amplification, clear up to the audio range”; “We should tell Shockley what we did today”; Bardeen to Jane peeling carrots: “We discovered something today”; December 23, 1947 executive demo, circuit “actually spoken over”; Shockley: “magnificent Christmas present” and “provoked conflicting emotions in me”; Shockley’s separate credit talks: “sometimes the people who do the work don’t get the credit for it” / Brattain: “Oh hell, Shockley, there’s enough glory in this for everybody”; Shockley’s solo month; January 23, 1948 junction conception; June 30, 1948 New York press conference; NYT July 1, 1948 “News of Radio” page below a soap opera sponsor; Pierce’s naming from trans-resistance; Western Electric point-contact production from 1951, >6,000/month by mid-1952 for telephone switching and hearing aids; Sonotone 1010 (1952) first commercial hearing aid with a transistor; July 4, 1951 junction announcement; “no pictures of Bardeen and Brattain without his presence” publicity order. URL: https://computerhistory.org/blog/the-surface-state-job/

H22 - NobelPrize.org, “John Bardeen - Facts”

Read: FULL (web page, 2026-11-01) Supports: Bardeen born 23 May 1908, Madison WI; died 30 January 1991, Boston MA; affiliation at 1956 award: University of Illinois, Urbana; prize motivation and 1/3 share; “Also awarded: Nobel Prize in Physics 1972.” URL: https://www.nobelprize.org/prizes/physics/1956/bardeen/facts/

P1 - Watzinger, Fackler, Nagler, Schnitzer, “How Antitrust Enforcement Can Spur Innovation: Bell Labs and the 1956 Consent Decree” (American Economic Journal: Economic Policy; online appendix PDF)

Read: EXCERPT (appendix history section, 2026-11-01) Supports: AT&T in 1956: largest private corporation in the world by assets; 746,000 employees; $5.3B revenue = 1.9% of US GDP; Bell Labs 1950 staff 6,000, one-third professional scientists/engineers = ~1% of US S&E workforce; 1940-1970 Bell filed ~503 patents/year (~1% of US patents); antitrust complaint filed January 1949; lawsuit frozen early 1952 with DoD support (Korea war effort); January 1953 Bell lobbied Eisenhower administration for dismissal on national-defense grounds; June 1954 AT&T concessions memo - major remedy offered: compulsory licensing of all Bell patents at reasonable royalties; Defense Secretary Wilson: severing Western Electric “contrary to the vital interests of the Nation”; consent decree January 24, 1956: (1) all Bell patents issued before the decree licensed royalty-free to any applicant (except RCA/GE/Westinghouse under B-2 cross-licenses), subsequent patents at reasonable royalties - 7,820 patents, 266 USPC classes, 1.3% of all unexpired US patents; (2) Bell barred from any business other than telecommunications; Judge Barnes: “[t]he patent relief in itself opens wide the door to hundreds of small businesses.” URL: https://assets.aeaweb.org/asset-server/files/13359.pdf

P2 - Nagler, Schnitzer, Watzinger, “Fostering the Diffusion of General Purpose Technologies: Evidence from the Licensing of the Transistor Patents” (Journal of Industrial Economics discussion paper, Nov 15, 2021)

Read: EXCERPT (abstract + introduction of discussion paper; substantial verbatim search excerpts of the published version, Journal of Industrial Economics 2022, doi:10.1111/joie.12311; 2026-11-01) Supports: transistor as defining general purpose technology; Bell Solid State Physics Group filed 166 transistor patents, 110 published by 1952 (“transistor patents”); transistor diffusion and cross-technology spillovers increased dramatically after AT&T began licensing its transistor patents with symposia to educate follow-on inventors in 1952; both symposia and licensing played important roles; a subsequent royalty reduction produced no further increase - licensing and technology transfer mattered more than royalty rates; contrast cases: Watt steam-engine patent, Wright brothers patent war as alleged blockers. Additional terms from the published version: $25,000 was a non-refundable ADVANCE against future royalties; royalty 5% of net selling price in 1950, reduced to 2% in 1953; more than 30 companies licensed after the April 1952 symposium; Bell waived all patent royalties on hearing-aid applications in homage to Alexander Graham Bell; licensing read in the literature as partly appeasing the 1949 DOJ antitrust suit, with internal memos also expecting reciprocal learning. URL: https://epub.ub.uni-muenchen.de/77870/1/297.pdf

T1 - Computer History Museum, “1951: Development of Zone Refining” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: zone refining (Pfann, 1950-51) reaches impurity levels of one part in ten billion (CHM analogy: “a pinch of salt in three freight cars of sugar”); method: repeated passage of a germanium-filled tube through heating coils, impurities swept to the ends in the molten zone; silicon unsuited: melts at 1415C vs germanium 937C and reacts with almost all materials; Theurer’s float-zone variation from 1952: vertical rod clamped at both ends, molten segment held by surface tension; steam refining to remove boron; silicon below one part per billion by early 1955; independent developments: Keck & Golay at US Army Signal Corps Fort Monmouth, and R. Emeis under Eberhard Spenke at Siemens, Pretzfeld, West Germany; primary refs: Pfann “Principles of Zone Melting” (July 1952), Theurer patent filed Dec 17, 1952. URL: https://www.computerhistory.org/siliconengine/development-of-zone-refining/

T2 - Computer History Museum, “1954: Silicon Transistors Offer Superior Operating Characteristics” (Silicon Engine)

Read: FULL (web page, 2026-11-01) Supports: first six years all transistors germanium; germanium easier to work with and allows higher-frequency operation BUT far worse leakage currents in “off” state (“an anathema for computer logic”) and restricted to 0-70C operation; silicon devices possible from -55 to 125C after DuPont began supplying high-purity semiconductor-grade material; January 1954 Morris Tanenbaum (Bell Labs) fashioned first silicon transistor (grown-junction variation); Bell did not pursue commercially; Teal had left Bell to organize TI research lab, hired Willis Adcock’s team; TI’s first silicon n-p-n grown-junction transistor April 14, 1954 using DuPont silicon; Teal (unaware of Tanenbaum) presented May 10, 1954 at IRE conference in Dayton, announcing silicon transistors in production and for sale - sensation; TI dominated silicon-transistor market for the next few years, cut into Raytheon’s position as largest merchant-market transistor supplier; by end of the 1950s silicon the industry’s preferred material; primary refs: Tanenbaum notebook Jan 26, 1954; Adcock et al. Proc. IRE July 1954. URL: https://www.computerhistory.org/siliconengine/silicon-transistors-offer-superior-operating-characteristics/

T3 - PBS “Transistorized!”, “The First Silicon Transistor” (1954)

Read: FULL (web page, 2026-11-01) Supports: IRE conference scene, late afternoon; speakers dismissing silicon transistor prospects for years; Teal: “Contrary to what my colleagues have told you about the bleak prospects for silicon transistors, I happen to have a few of them here in my pocket”; germanium’s thermal failure mode (heat frees too many carriers); Teal began growing silicon crystals at Bell in 1950; April 14, 1954 Teal showed TI VP Pat Haggerty a working silicon transistor; four weeks later production already started; “the first company to produce a truly consistent mass-produced transistor.” URL: https://www.pbs.org/transistor/science/events/silicont1.html

T4 - Royal Society of Chemistry periodic table, silicon element page

Read: SEARCH SNIPPET + element page content (2026-11-01) Supports: silicon makes up 27.7% of Earth’s crust by mass and is the second most abundant element (oxygen first); does not occur uncombined; chiefly as oxide (silica - sand, quartz, rock crystal) and silicates. Limitations: RSC educational page; the percentage is a standard crustal-abundance figure (other tabulations give ~28%). URL: https://periodic-table.rsc.org/element/14/silicon

T5 - U.S. Geological Survey, “Mineral resource of the month: silicon”

Read: SEARCH SNIPPET (2026-11-01) Supports: silicon the second most abundant element in Earth’s crust, more than 25 percent of the crust by weight; USGS framing of silicon as mineral commodity. Limitations: snippet-level read; supports only the crustal-abundance claim. Not cited in the text; retained as a consulted source. URL: https://www.usgs.gov/publications/mineral-resource-month-silicon

P3 - Chenming Hu (UC Berkeley), “Electrons and Holes in Semiconductors” (textbook chapters 1-3, PDF)

Read: SEARCH SNIPPET + chapter text via search (2026-11-01); full PDF not yet read cover to cover Supports: silicon band gap about 1.1-1.12 eV; Table 1-1 band gaps: Ge 0.67, Si 1.12, GaAs 1.42 eV; thermal energy kT is 26 meV at room temperature - far below both gaps but exponentially nearer germanium’s, hence germanium’s much larger thermally generated carrier population; Hu is the Berkeley device-physics authority (BSIM, FinFET pioneer). URL: https://www.chu.berkeley.edu/wp-content/uploads/2020/01/Chenming-Hu_ch1-3.pdf

P4 - “Properties of Silicon and Germanium” (CRC/Taylor & Francis chapter, doi:10.1201/b13001-80)

Read: SEARCH SNIPPET + data tables via search (2026-11-01) Supports: room-temperature intrinsic carrier density: silicon 1.02x10^10 cm-3 vs germanium 2.33x10^13 cm-3 (~2000:1 - the physical basis of germanium’s leakage); band gaps Si 1.12 eV (300 K), Ge 0.664 eV (291 K); electron/hole mobilities (Ge higher). Limitations: data-table chapter read via search excerpt; its melting-point row for Ge looked mislabeled in the excerpt, so this source is cited only for band gap and carrier density, not thermal data. URL: https://doi.org/10.1201/b13001-80

M2 - von Ammon & Eyer (TU Munchen / Uni Kiel), “Czochralski’s Creative Mistake: A Milestone on the Way to Advanced Silicon Crystal Growing” (PDF)

Read: SEARCH SNIPPET + sections via search (2026-11-01) Supports: about 95% of world silicon single-crystal production by the Czochralski method; modern CZ crystals up to 2 m long, 300 mm diameter, ~265 kg; wafer diameter timeline (industrial 50 mm in the 1970s, 100 mm in 1980, 200 mm by 1995, 300 mm by 2002); 300-mm pull takes 3-4.5 days, drawing rate 0.4-1.2 mm/min, melt charge ~300 kg under argon; silica crucible supported by graphite; dislocation-free “necking” step; suppliers named: Shin-Etsu, Sumco (Japan), Wacker-Chemie (300-mm wafers outside Japan); Jan Czochralski’s original 1916 discovery. Limitations: mid-2000s paper - 450 mm forecasts dated; use for process and timeline, not current-state forecasts. URL: https://www.tf.uni-kiel.de/matwis/amat/iss/kap_6/articles/growing_si_crystals.pdf

P5 - ScienceDirect Topics, “Purity Polysilicon” (chapter summary)

Read: SEARCH SNIPPET + chapter text via search (2026-11-01) Supports: chain from metallurgical-grade silicon (98%, from quartz reduced with carbon in an electric furnace) through trichlorosilane synthesis, distillation, and CVD decomposition onto seed rods (Siemens route) to high-purity polysilicon; solar-grade 6N (99.9999%); electronic-grade 9N to 11N (99.999999999%); polysilicon broken into chunks as crystal-growth feedstock. URL: https://www.sciencedirect.com/topics/engineering/purity-polysilicon

P6 - LibreTexts (Barron, Chemistry of the Main Group Elements), “Semiconductor Grade Silicon”

Read: SEARCH SNIPPET + page text via search (2026-11-01) Supports: metallurgical-grade silicon ~98%; EGS carbon/oxygen under a few ppm, metals at ppb or lower; typical EGS impurity table (boron <=0.1 ppb, phosphorus <=0.3 ppb, iron 0.1-1.0 ppb, gold <0.00001 ppb); EGS “one of the purest materials commonly available”; silicon ~28% of crust, second after oxygen (46%). URL: https://chem.libretexts.org/Bookshelves/Inorganic_Chemistry/Chemistry_of_the_Main_Group_Elements_(Barron)/07%3A_Group_14/7.10%3A_Semiconductor_Grade_Silicon

M3 - MDPI Eng Proc., “Electronic-Grade Silicon (EG Si) Wafer Production: Review and Update of Life Cycle Inventory Data” (2026)

Read: SEARCH SNIPPET + abstract/sections via search (2026-11-01) Supports: 9N = 99.9999999% = 1 ppb impurity; 11N = 99.999999999% = 0.01 ppb; EG Si wafers 11-13 N (CEA-Leti R&D range), 200-300 mm, 725-775 um thick; polysilicon purification, CZ pulling and wafer slicing are the most energy-intensive supply-chain stages. URL: https://www.mdpi.com/2673-4591/127/1/16

M4 - Computer History Museum, “1955: Development of Oxide Masking” (Silicon Engine)

Read: FULL page text via search result (2026-11-01); direct fetch failed (crawler timeouts) - content captured complete in search excerpt Supports: early 1955 pitting problem on silicon wafers during high-temperature diffusion; Frosch’s serendipitous accident - hydrogen carrier gas briefly caught fire, introducing water vapor, coating wafers with glassy SiO2; developed with technician Lincoln Derick; established which impurities penetrate the oxide (gallium could; boron and phosphorus could not); etched small openings to diffuse selected areas, patterning precise n- and p-type regions; patented and published 1957 (J. Electrochem. Soc. 104(9):547-552; US Patent 2,802,760 issued Aug 13, 1957); oxide later essential to planar processing (1959) as junction protection and as insulation under metal interconnects; “more than any other single factor, silicon’s oxide layer has established it as the dominant material in microchip manufacturing.” CONFLICT NOTED: filing date of patent 2,802,760 - CHM says filed Dec 2, 1956; BLTJ 1997 (M5) says Dec 2, 1955. Avoid the filing year in prose; use issue date. URL: https://www.computerhistory.org/siliconengine/development-of-oxide-masking/

M5 - Michael Riordan, “Key Steps to the Integrated Circuit” (Bell Labs Technical Journal, Autumn 1997)

Read: SEARCH SNIPPETS + long excerpts via search (2026-11-01); full PDF located at memorial.bellsystem.com Supports: Fuller 1952 controlled diffusion of dopants to shallow depths (Phys. Rev. 86:136); Lee 1954 first diffused-base germanium mesa transistor, cutoff 500 MHz, ~10x the best alloy transistors (BSTJ Jan 1956); Frosch & Derick 1955 oxide masking with windows; Andrus & Bond photoresist on oxide preventing etch - optical exposure through photomasks creates precise window patterns (Andrus patent filed Aug 15, 1957); Tanenbaum & Thomas 1955 all-diffused silicon transistor (BSTJ Jan 1956), announcement “created great excitement throughout the infant industry”; mesa construction detail (wax masking, acid etch, raised mesa) and its fatal weakness - exposed junctions vulnerable to dust, residues, fingerprints, causing reliability problems and yield loss; Hoerni’s planar solution: oxide left over junctions, repetition of oxide-grow/pattern/diffuse steps; Shockley left Bell 1955 for Palo Alto; 1957 eight led by Noyce left to form Fairchild; Fairchild landed IBM order for diffused mesa transistors; profitable within two years, revenues over half a million dollars; epitaxy reference (Theurer, Kleimack, Loar, Christensen,

“Epitaxial Diffused Transistors,” Proc. IRE Sept 1960); Atalla, Tannenbaum, Scheibner “Stabilization of Silicon Surfaces by Thermally Grown Oxides.” URL: https://memorial.bellsystem.com/pdf/bell_labs_journals/bell_labs_technical_journal_autumn_1997_2.pdf

M7 - Computer History Museum, “1959: Practical Monolithic Integrated Circuit Concept Patented” (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: patent attorney John Ralls challenged Noyce to find other uses for planar; Noyce conceived monolithic IC: diodes, transistors, resistors, capacitors diffused into silicon, interconnected by aluminum lines deposited atop the oxide; eliminating “flying wires” made Kilby’s solid circuits manufacturable; Noyce patent filed July 30, 1959 (US 2,981,877, issued April 25, 1961); first working monolithic ICs May 1960; isolation eventually by reverse-biased p-n junction (Kurt Lehovec, Sprague Electric, patent filed April 22, 1959); Fairchild-TI litigation for years; courts ruled for Noyce but cross-license with net payment to Fairchild already settled; Kilby and Noyce co-celebrated: Kilby first working all-semiconductor circuit, Noyce the metal-over-oxide interconnection; Noyce died 1990, did not share Kilby’s 2000 Nobel. URL: https://www.computerhistory.org/siliconengine/practical-monolithic-integrated-circuit-concept-patented/

M8 - Computer History Museum, “1960: First Planar Integrated Circuit is Fabricated” (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: August 1959 Noyce asked Jay Last to develop the IC; team: Sam Fok, Isy Haas, Lionel Kattner, James Nall; Don Farina characterization data; Robert Norman designed a four-transistor, five-resistor flip-flop in modified DCTL; first working monolithic devices May 26, 1960 with epoxy-filled etched-channel isolation; boron-diffusion p-n junction isolation (Haas & Kattner) working circuits September 27, 1960; Micrologic type “F” flip-flop announced March 1961 at IRE Show New York with LIFE magazine photograph; five more circuits (incl. type “G” gate) in October 1961; TI announced Series 51 DCTL IC family October 1961, its first with deposited-metal interconnects. URL: https://www.computerhistory.org/siliconengine/first-planar-integrated-circuit-is-fabricated/

M9 / M16 / M20 - Computer History Museum, “The Fairchild Chronicles” timeline (archive PDF)

Read: SEARCH SNIPPETS + section excerpts covering 1958-1959, 1963, 1966-1968, 1987 (2026-11-01) Supports: Hoerni patent disclosure January 14, 1959 (Lecuyer: “the most important innovation in 20th century technology”); first planar transistor demonstrated March 12, 1959 (Hoerni proved contamination resistance by spitting on the unpackaged die); Noyce’s monolithic ideas written late January 1959; Kilby September 1958 first integrated flip-flop (two mesa transistors gold-wire connected on germanium); TI announced Kilby’s “Solid Circuit” at March 1959 IRE show, spurring Noyce/Last; Rheem Semiconductor first Fairchild spin-out March 1959 (Ed Baldwin + eight senior employees; Noyce appointed GM); 2N706 first gold-doped transistor May 1959 (16 ns switching, 3x smaller than 2N696); Minuteman program used Fairchild 2N1132 among others; Last’s September 1959 “Hexistor” multi-chip demo for Wescon. Supports (1963): October 1963 Ed Snow identified sodium as the major source of MOS drift/contamination, enabling reliable LSI; July 1963 Andrew Grove joined Fairchild R&D under C. T. Sah, collaborating with Bruce Deal and Ed Snow on MOS; 1963 NEC exclusive license for Fairchild planar/IC patents in Japan (Noyce-assisted, Borovoy negotiated); Hong Kong assembly plant exploration 1963, board approval 1964, within a year Fairchild the largest electronics employer in Hong Kong; General Micro Electronics founded 1963 by Norman, Ferguson, Bobb, later hired Wanlass, first commercial MOS products; Fairchild 1963 microcircuit sales 183,000 units for $3.8M against industry total of $15.8M. Supports (1966-1968, 1987): peak mid-1960s - one of the world’s largest silicon-transistor producers, over 30 percent of the IC market; starved by parent for investment funds and stock equity for key employees; October 1967 first loss since 1958 (industry downturn + manufacturing difficulties + share loss to TI SN7400 TTL); Semiconductor by then >50% of corporate sales; CEO John Carter fired, replaced by Richard Hodgson; Charlie Sporck resigned March 1967 to National Semiconductor (frustrated by low investment and no stock options), taking senior managers incl. Pierre Lamond - “seriously damaged Fairchild’s manufacturing capability”; Univac order September 1967 - 3 million custom ICs, about $7M; 9300 TTL-MSI shift register September 1967; February 1968 Hodgson removed, Noyce passed over for top job, approached Moore about a memory company; Noyce resigned June 25, 1968 (“get close to advanced technology again”); Moore resigned July 3; NM Electronics incorporated July 18, 1968, soon renamed Intel; investors included five Fairchild founders and Arthur Rock as chairman; Hogan’s Motorola team arrived August 12, 1968; Jerry Sanders fired 1968, co-founded AMD July 1969; uA741 op-amp May 1968 (Dave Fullagar) “most popular op-amp of all time”; 3801 first standard MOS-LSI product May 1968; Faggin’s first commercial silicon-gate MOS IC October 1968 (SGS-Fairchild assignment); 1967 financials: net sales $196,952,000, net loss $7,547,000, 19,385 employees. CONFLICT NOTED: this timeline dates Sanders’ co-founding of AMD to July 1969, but AMD’s own corporate history and multiple independent chronologies date the founding to May 1, 1969 - treat May 1, 1969 as the founding date. Note: three section-level registrations of the same archive PDF merged; [M16] and [M20] citations resolve here. URL: http://archive.computerhistory.org/resources/access/text/2012/10/102746515-05-01-acc.pdf

M10 - NobelPrize.org educational, “The History of the Integrated Circuit”

Read: SEARCH SNIPPETS + page text via search (2026-11-01) Supports: “tyranny of numbers” explained for general readers (manual soldering of vast component counts impossible without faulty connections; wire length limited computer speed); Kilby newly employed, no vacation, worked alone in summer 1958; monolithic idea - all components and chip from the same block of semiconductor; September 1958 first IC tested and worked; metal connections as a layer on top removes manual assembly; manufacturability/automation point. URL: https://educationalgames.nobelprize.org/educational/physics/integrated_circuit/history/index.html

M11 - Computer History Museum, “Revolution: The Integrated Circuit” (story page)

Read: SEARCH SNIPPETS (2026-11-01) Supports: Kilby's first working circuit tested September 12, 1958, etched on germanium; Kilby's remark that if he had known he'd be showing it for the rest of his life he would have "prettied it up a little"; hired to design transistor circuit modules, judged modules a dead end; fine gold "flying wires" connected oscillator/amplifier solid circuits; TI introduced the Type 502 Binary Flip-Flop in 1959; hand-crafted approach impractical for mass production but pointed the way. URL: https://www.computerhistory.org/revolution/story/276

M12 - IEEE Pikes Peak Section, "Who Invented the Integrated Circuit?" (PDF presentation)

Read: SEARCH SNIPPET (2026-11-01) Supports: J. A. Morton (Bell Labs VP) in Proceedings of the IRE, 1958: systems "require hundreds, thousands, and sometimes tens of thousands of electron devices. Each element must be made, tested, packed, shipped, unpacked, retested, and interconnected one-at-a-time to produce a whole system" - the canonical "tyranny of numbers" statement. URL: https://site.ieee.org/pikespeak/files/2020/06/Invention-of-the-Integrated-Circuit-Distribution-Final.pdf

M13 - Kansas Historical Society, Kansapedia, "Jack St. Clair Kilby"

Read: SEARCH SNIPPET (2026-11-01) Supports: Kilby joined TI May 1958, microminiaturization at his own request; no accrued vacation, worked alone during July shutdown; September 12, 1958 demonstration; patented February 6, 1959; patent text: "a body of semiconductor material ... wherein all the components of the electronic circuit are completely integrated." URL: https://www.kansashistory.gov/kansapedia/jack-st-clair-kilby/12125

M14 - Computer History Museum, "1960: Metal Oxide Semiconductor (MOS) Transistor Demonstrated" (Silicon Engine) + People entries for Atalla and Kahng

Read: FULL page texts via search results (2026-11-01) Supports: 1959 Atalla & Kahng at Bell achieved first successful insulated-gate FET by overcoming surface states (anticipated by Lilienfeld, Heil, Shockley); thermally grown SiO2 markedly reduces interface states; metal-oxide-semiconductor sandwich; device slow and unneeded by telephony, not pursued at Bell; Kahng's January 1961 memo noted "ease of fabrication and the possibility of application in integrated circuits"; RCA's Zaininger & Meuller built MOS in 1960, Sah built an MOS tetrode at Fairchild, Heiman & Hofstein built a 16-transistor experimental MOS IC at RCA in 1962; commercial MOS 1964 (GME 1004, Fairchild FI 100 p-channel; RCA 3N98 n-channel amplifier); n-channel faster but harder to make; "over 99 percent of microchips produced today use MOS transistors"; Kahng patent US 3,102,230 filed May 31, 1960; Atalla et al. "Stabilization of Silicon Surfaces by Thermally Grown Oxides," BSTJ May 1959; Atalla biography (Port Said, Purdue doctorate 1949, later Atalla Corporation banking security); Kahng biography (Seoul-born, Ohio State PhD, joined Bell 1959, later flash-memory contributions). URL: https://www.computerhistory.org/siliconengine/metal-oxide-semiconductor-mos-transistor-demonstrated/

M15 - Computer History Museum, "1963: Complementary MOS Circuit Configuration is Invented" (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: 1963 ISSCC paper by Sah & Wanlass (Fairchild R&D): complementary p-channel + n-channel pairs draw close to zero standby power; Wanlass patent US 3,356,858 filed June 18, 1963; RCA pioneered production CMOS (COS/MOS), Herzog's 1965 Air Force computer program, 1968 288-bit SRAM and CD4000 family, 1975 COSMAC 1802 (Chrysler engine controllers); first high-volume CMOS uses were battery products (digital watches) not demanding speed; by 1978 (Masuhara, Hitachi, ISSCC high-speed CMOS RAM) smaller lithography + silicon-gate process let CMOS compete with bipolar and conventional MOS; as scaling packed hundreds of thousands of transistors per chip, CMOS was the best answer to power density. URL: https://www.computerhistory.org/siliconengine/complementary-mos-circuit-configuration-is-invented/

L1 - John H. Bruning, "Optical Lithography: 40 Years and Holding" (2007, lithoguru.com PDF)

Read: SEARCH EXCERPTS (2026-11-01) Supports: contact/proximity printing lineage from printing industry (Rubylith masters, pattern generators, step-and-repeat mask cameras); contact printing damages wafer and mask with each use; Perkin-Elmer 1970 all-reflective 1:1 scanning system (Micralign 100, Offner relay), changed the landscape for a decade, NA limited ~0.16; overlay rule of thumb: layer-to-layer overlay error <= 20% of minimum critical dimension; wafer growth 50->75mm strained 1:1 masks (capped at 6-inch); Bell Labs EBES electron-beam mask writers commercialized early 1980s; GCA 4800 DSW (1978) first wafer stepper with automated handling/alignment, Zeiss 10:1 reduction lens, NA 0.28, 10x10 mm field, mercury g-line 436 nm. URL: https://www.lithoguru.com/scientist/litho_history/Optical_lithography_40_years_and_holding_Bruning_2007.pdf

L2 - Atsuhiko Kato, lithography history presentation (lithoguru.com PDF)

Read: SEARCH EXCERPTS (2026-11-01) Supports: 1965 Kulicke & Soffa first commercial contact aligners, near-100% of the (small) 1960s market; 1973 Perkin-Elmer Micralign projection scanner (NA 0.167, R&D from 1969 under Wright-Patterson Air Force Base contract) - projection + positive resist dramatically cut defect rates, made P-E the industry's largest tool firm; 1978 GCA DSW 4800 first successful wafer stepper (g-line, 10x, Zeiss 0.28 NA, 10x10 mm field), an extension of the D.W. Mann photorepeater, early customers IBM/AT&T/Fairchild/National/Siemens; low throughput vs projection initially; the 256K DRAM generation made steppers the mainstream tool; Nikon NSR-1 prototype 1978 funded by the NTT/MITI VLSI Research Program (1976). URL: https://www.lithoguru.com/scientist/litho_history/Kato_Litho_History.pdf

L3 - chiphistory.org, "Lithography tool and competitive transition history"

Read: SEARCH SNIPPET (2026-11-01) Supports: the projection-to-stepper transition was arguably more tumultuous than EUV; proximity aligner evolved from contact aligner; IBM and Philips tried and failed at stepper-like conversion in the early 1970s; Perkin-Elmer Micralign (1973) “put the stepper on an indefinite hold” for a time. Limitations: community history site; use for color, not sole support of load-bearing dates. URL: https://www.chiphistory.org/750-lithography-tool-and-competitive-transition-history

M17 - Computer History Museum, “Silicon Comes to Silicon Valley” (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: September 1955 Shockley and Arnold Beckman agree to found Shockley Semiconductor Laboratory as a Beckman Instruments division; building at 391 South San Antonio Road, Mountain View; recruiting goal “the most creative team in the world for developing and producing transistors”; December 1956 Nobel; staff disenchantment with difficult management; preference for immediate silicon-transistor opportunities vs the distant four-layer p-n-p-n diode (conceived for telephone switching); failed appeal to Beckman for a new manager; September 1957 resignation of eight - Blank, Grinich, Hoerni, Kleiner, Last, Moore, Noyce, Roberts - founding Fairchild Semiconductor in Palo Alto; many others followed; Shockley’s firm never profitable, sold to Clevite 1960; Shockley became Stanford professor. URL: https://www.computerhistory.org/siliconengine/silicon-comes-to-silicon-valley/

M18 - Computer History Museum archive monograph on the planar process and Fairchild founding (2017 PDF, drawing on Riordan/Crystal Fire and Lecuyer)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Shockley set up a secret separate R&D group on the four-layer diode; mid-May 1957 Beckman meeting blowup - Shockley stormed out shouting “If you don’t like what we’re doing here, I can take this group and get support any place else!”; Shockley notebook: “Wed 18 Sep - Group resigns”; $1.38 million agreement brokered by Hayden Stone with Fairchild Camera and Instrument; the eight had read the Frosch & Derick preprint while still at Shockley Lab - head start on double diffusion and oxide masking (per Roberts: Hoerni, Moore, Noyce experimenting); first Fairchild product aimed at IBM’s B-70 bomber guidance computer (core-memory driver transistor); division of labor: Roberts crystals, Moore diffusion, Last & Noyce oxide masking and photolithography incl. a step-and-repeat camera; May 1958 n-p-n mesa prototypes; first commercially successful mesa transistors, ahead of TI; 1958 sales over $500,000, almost all from that product, year ended in the black. URL: https://archive.computerhistory.org/resources/access/text/2017/01/102770281-05-01-acc.pdf

M19 - Computer History Museum blog, “Fairchild Semiconductor: The 60th Anniversary of a Silicon Valley Legend”

Read: SEARCH SNIPPET (2026-11-01) Supports: September 19, 1957 the eight signed papers establishing Fairchild Semiconductor; Arthur Rock assisted; Rock later formed one of the first West Coast venture-capital firms; post-Sputnik military urgency for miniaturized, reliable aerospace electronics framed the market opening. URL: https://computerhistory.org/blog/fairchild-semiconductor-the-60th-anniversary-of-a-silicon-valley-legend/

M21 - Los Angeles Times, “Schlumberger Will Sell Its Ailing Fairchild Unit” (September 1, 1987)

Read: SEARCH SNIPPET (2026-11-01) Supports: National Semiconductor agreed to buy Fairchild from Schlumberger for $122 million, called “a steal,” about half what Fujitsu had offered for an 80% stake earlier in 1987 - that deal collapsed amid US government opposition on national-security grounds; Schlumberger paid $425 million in 1979 and expected to lose another $220 million on the sale; Fairchild “the birthplace of the integrated circuit” and “a fount of semiconductor industry talent and technology.” CONFLICT NOTED: Wikipedia’s Fairchild article says $200M sale price; the contemporaneous LA Times says $122M - use LA Times. URL: https://www.latimes.com/archives/la-xpm-1987-09-01-fi-5326-story.html

M22 - Computer History Museum, Fairchild Oral History Panel, “The Legacy of Fairchild” (Fairchild at 50, PDF)

Read: EXCERPT (panel transcript PDF, Moore/Sanders/Corrigan sections read in full, 2026-11-01) Supports: Gordon Moore’s own account - he initially declined Noyce (“I’ve got the best job in the industry”) but followed when he learned Noyce was leaving and outside management was coming in; Jerry Sanders’ account of Sporck’s resignation and Syosset corporate management friction - Sporck told Sanders “I just can’t work here any more” and “took, basically, all of the key manufacturing managers” to National, which became a manufacturing powerhouse (Widlar had recruited Sporck); Wilf Corrigan’s account that Intel’s founding then ripped out a second wave of the original management, leaving “a certain amount of chaos”; Sanders joined Fairchild in 1961 at age 24 as Los Angeles district sales manager, hired out of Motorola. URL: https://archive.computerhistory.org/resources/text/Oral_History/Fairchild_at_50/102658284.05.01.acc.pdf

I4 - IEEE Spectrum, “The First Transistor Radio: Engineering the Regency TR-1” (2024, 70th anniversary)

Read: SEARCH EXCERPTS (2026-11-01) Supports: May 21, 1954 Haggerty challenged a TI research group for a working radio prototype within a week - breadboard with eight transistors in four days; Haggerty committed $2 million, just under 10% of TI revenue; partner IDEA (Indianapolis) signed June 1954, Regency brand; final design battery cost about $1.25, 20-30 hours playing life); announced October 18, 1954, on sale November 1 in New York and Los Angeles; sold 100,000 in first year; never very profitable; Haggerty estimated it pushed the transistorized consumer market ahead by two years; Bell Labs

licensing at $25,000 through Western Electric from 1951 - Haggerty bought TI's license in 1952 (CORROBORATES the license-fee figure from an independent source). URL: https://spectrum.ieee.org/transistor-radio-invented

I5 - Texas State Historical Association, Handbook of Texas, "Texas Instruments"

Read: SEARCH EXCERPTS (2026-11-01) Supports: origins - Karcher & McDermott's Geophysical Research Corporation (Tulsa, 1924, Amerada subsidiary), moved to Dallas 1930 as Geophysical Service Inc.; WWII submarine-detection electronics; Haggerty joined 1945; renamed Texas Instruments 1951, NYSE 1953; Teal hired 1952; first portable transistor radio 1954; silicon transistors 1954 (Adcock team); 1956 total sales $45 million vs $3 million in 1946; led the industry in transistor sales; by late 1953 mass-producing germanium transistors under Mark Shepherd Jr. (per TSHA's Haggerty entry). URL: https://www.tshaonline.org/handbook/entries/texas-instruments

I6 - Computer History Museum, "1963: Standard Logic IC Families Introduced" (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: DTL first high-volume IC product lines - Signetics SE100 (Orville Baker, 1962) overtaken by Fairchild 930 Series (1964); TTL patented by James Buie of Pacific Semiconductor (1961); Sylvania SUHL first TTL family 1963 (Thomas Longo; Hughes Phoenix missile win); TI SN5400 military TTL family 1964; SN7400 in low-cost plastic packages for industrial customers 1966, quickly over 50% of the logic market; 1968 TTL-MSI (Fairchild 9300, Signetics 8200). URL: https://www.computerhistory.org/siliconengine/standard-logic-ic-families-introduced/

I7 - Computer History Museum blog, "The Rise of TTL: How Fairchild Won a Battle But Lost the War"

Read: SEARCH SNIPPET (2026-11-01) Supports: TI's SN5400 replicated Sylvania circuits in a TI process (design manager Jerry Luecke); SN7400 plastic DIP 1966 opened the industrial market; National (ex-Fairchild management) second-sourced; TI copied Fairchild MSI devices under 74xx numbers (9300 -> 74195, 9341 -> 74181); Fairchild became second-largest TTL maker, but TI stayed dominant and most profitable with over 50% of a worldwide market that reached $750 million in 1975. URL: https://computerhistory.org/blog/the-rise-of-ttl-how-fairchild-won-a-battle-but-lost-the-war/

M23 - Computer History Museum, "1970: MOS Dynamic RAM Competes with Magnetic Core Memory on Price" (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: Schmidt 64-bit p-channel SRAM at Fairchild 1964; Karp's dynamic clocking (GMe) -> Boysel 256-bit DRAM Fairchild 1968, 1K/2K at Four Phase 1969; Honeywell's Regitz proposed 3-transistor cell, implemented by Karp in Intel's p-channel silicon-gate process; improvements by Ted Hoff, design Bob Abbott, debug Bob Reed -> the 1103; priced at 1 cent/bit, from 1970 quickly replaced magnetic core main memory; IBM committed to the process on System/370 Model 158 in 1972; Mostek Proebsting MK4096 4K in 16-pin package 1973; 16K MK4116 1976 adopted Dennard's patented single-transistor cell + Stein (Siemens) design methods; 64K DRAMs from Japanese and US vendors before decade's end. URL: https://www.computerhistory.org/siliconengine/mos-dynamic-ram-competes-with-magnetic-core-memory-on-price/

M24 - Computer History Museum, "1971: Microprocessor Integrates CPU Function onto a Single Chip" (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: late-1960s race to CPU-on-LSI; Boysel's Four-Phase AL-1 8-bit CPU slice 1969; Geller & Holt MP944 F-14A Central Air Data Computer chipset (Garrett AiResearch, AMI fabrication, 1970); Hoff & Mazor conceived the 4004 4-bit CPU within the MCS-4 chip set; 1971 Faggin, assisted by Masatoshi Shima, used silicon-gate MOS to fit 2300 transistors in a 16-pin package; 8008 announced 1972 (Faggin supervising Hal Feeney; designed for CTC/Datapoint; TI's TMX1795 prototype never offered commercially); 8080 and Motorola 6800 (Tom Bennett) 1974 established the MPU; MOS Technology 6502 enabled Apple/Atari/Commodore; Zilog Z80; 16-bit mid-1970s; 8086/8088 in IBM PC and 68000 in Macintosh. URL: https://www.computerhistory.org/siliconengine/microprocessor-integrates-cpu-function-onto-a-single-chip/

M25 - Computer History Museum, "1968: Silicon Gate Technology Developed for ICs" (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: Kerwin, Klein, Sarace at Bell Labs replaced aluminum gate with polycrystalline silicon 1967 (self-aligned, faster, denser, more reliable); Watkins described similar structure at GMe 1965, patent delayed to 1969; Faggin with Tom Klein at Fairchild commercialized it - first silicon-gate IC Fairchild 3708 (1968); Intel's first commercial MOS device the 1101 256-bit RAM 1969; silicon-gate delivered 3-5x speed in half the chip area; Faggin joined Intel 1970, added buried contact, made the 4004 fit a manufacturable die; enabled economical EPROM (1971); within five years silicon-gate MOS was the industry standard, displacing bipolar except at the highest speeds. URL: https://www.computerhistory.org/siliconengine/silicon-gate-technology-developed-for-ics/

I9 - Junjiro Shintaku et al., "Technology Transfer as a Dialogical Process Crossing the Pacific Ocean: Sony's Transistor Technology Transfer" (Historia Scientiarum 26(2), academic PDF)

Read: SEARCH EXCERPTS (2026-11-01) Supports: WE transistor license fee $25,000 (further corroboration); Totsuko contracted WE October 1953 - first Japanese company with a WE transistor license; MITI foreign-currency approval came late 1953; trial manufacture of germanium point-contact and junction transistors by April 1954; Japan's first point-contact transistor made at ECL March 1953; Kobe Kogyo first trial manufacture of point-contact in Japan;

American engineers tried to dissuade Ibuka (transistors suitable for hearing aids, not radio-frequency amplification); Iwama (Morita's brother-in-law, later Sony's fourth president) led transistor R&D and toured US facilities; Totsuko exploited Bell-authored textbooks and the published zone-refining technique as shortcuts; TR-52 assembled January 1955 (five transistors), never sold (case deformation); TR-55 shown July 23, 1955 at Tokyo Kaikan; five in-house transistors (2T55/2T52/2T22/2T53/2T12 - grown-junction and alloy-junction types); priced 18,900 yen when a graduate civil servant earned 7,000-8,000 yen/month; transistor instability required selecting among 12 local oscillators per radio; early buyers rated sound below tube portables, but battery cost was 1/20th; sales surged among young people in summer 1956. URL: https://www.jstage.jst.go.jp/article/historiascientiarum/26/2/26_112/_pdf/-char/en

I10 - Sony Group official milestones, "Product & Technology Milestones - Radio" + Sony Semiconductor history page

Read: SEARCH EXCERPTS (2026-11-01) Supports: TR-55 the first product to bear the SONY logo (company renamed Sony only in January 1958); Totsuko "the first company in the world to make a radio using its own transistors"; 1954 Japan's first PNP alloy transistor prototype; TR-55 "rebirth of the radio as a portable device"; pre-transistor radio as large furniture the family gathered around. URL: https://www.sony.com/en/SonyInfo/CorporateInfo/History/sonyhistory-b.html

M26 - Computer History Museum blogs, "Who named Silicon Valley?" (2015) and "Silicon Valley Turns 50" (2021) + CHM scan of the Electronic News front page

Read: SEARCH EXCERPTS (2026-11-01) Supports: January 11, 1971 Electronic News ran Don Hoefler's three-part series on Fairchild and the Bay Area semiconductor industry under the headline "SILICON VALLEY U.S.A." - the first known appearance of the name in print; the phrase was already slang among industry salespeople ("that's what the guys call it," per colleague Jim Vincler's account); the paper's masthead wrongly carried 1970; region previously known as "Valley of Heart's Delight" for orchards; Hoefler's 1981 reflection: "made in a valley, from silicon - not silicone, please - the second most-abundant chemical element (after oxygen) on Earth"; the name quickly went industry-wide then generic worldwide; "Silicon Valley is not a place but a state of mind" attributed to John Doerr and Regis McKenna among others. URL: https://computerhistory.org/blog/who-named-silicon-valley/

M27 - Stanford Office of Technology Licensing, "Stanford Research Park" history paper (2004 PDF)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Industrial Park created to support a land-rich but cash-poor university; Varian first occupant (1953 per this paper; first ground lease October 1951 per Stanford Report); HP world HQ in the park 1956; more than 40 companies by 1960; Terman promoted to Provost 1955; Terman contacted Shockley in 1955 to locate his lab near Stanford; Shockley's company "the seed from which the Silicon Valley semiconductor industry grew"; by 1980 over 50 semiconductor companies in the valley directly linked to Shockley's startup; park's sharing/networking culture noted as a hallmark. URL: https://web.stanford.edu/group/OTL/documents/JSstanfordpark.pdf

M28 - AnnaLee Saxenian, "Creating a Twentieth Century Technical Community" (Frederick Terman paper)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Terman's role in Hewlett-Packard's founding - encouraged the students, lent them money, arranged a Palo Alto bank loan, helped sell patent rights; Terman promoted the Stanford Industrial Park as "our secret weapon"; Varian's late-1940s move to be near collaborators and graduate students. URL: https://people.ischool.berkeley.edu/~anno/Papers/terman.html

M29 - Sequoia Capital official history + HBS case abstract on Don Valentine

Read: SEARCH EXCERPTS (2026-11-01) Supports: Don Valentine - veteran salesman at Fairchild and National - founded Sequoia Capital in 1972; first $3 million fund backed Apple and Atari; Valentine's approach: bet on market size rather than founder pedigree or technology alone. URL: https://sequoiacap.com/our-history

M30 - Electronics Weekly, "How Kleiner Perkins Got Started, by Tom Perkins" (2008)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Kleiner & Perkins set up on Sand Hill Road in 1972 with an $8 million fund (fell short of a $10M target); half from Henry Hillman; Noyce and Moore each invested $200,000; Eugene Kleiner was one of the eight Fairchild founders; early floundering, then founding Tandem Computers themselves. Limitations: yarn-style retelling of Perkins' memoir; fine for color and the fund facts. URL: https://www.electronicsweekly.com/blogs/mannerisms/yarns/how-kleiner-perkins-got-starte-2008-04/

M31 - Ferrary & Granovetter, "The role of venture capital firms in Silicon Valley's complex innovation network" (Economy and Society, 2009) - via secondary citation

Read: CITATION SNIPPET ONLY (2026-11-01) Supports: Mayfield Fund founded 1969; Sequoia Capital and Kleiner, Perkins, Caufield & Byers followed in 1972; by 1975 more than thirty VC firms located in the Bay Area. Limitations: read only as quoted in another source; the underlying claim is uncontroversial and multiply echoed. URL: https://en.wikipedia.org/wiki/Sequoia_Capital

M32 - Computer History Museum, “1965: Moore’s Law Predicts the Future of Integrated Circuits” (Silicon Engine)

Read: FULL page text via search result (2026-11-01) Supports: Moore’s internal paper drew a line through five component-count points (1959-1964) for minimum cost per component; “The Future of Integrated Electronics” projected to 1975: 65,000 components per chip, doubling every 12 months; published as “Cramming more components onto integrated circuits,” Electronics, April 19, 1965; 1975 IEDM revision: projection realized via photolithography, wafer size, process technology, “circuit and device cleverness”; future rate slowed to a doubling every two years; the prediction became self-fulfilling - “Moore’s Law” dubbed by Carver Mead; 1995 Pentium nearly 5 million transistors; Moore 2003 paper titled “No Exponential Is Forever: but ’Forever’ Can Be Delayed!”; originally written to encourage customers to design in Fairchild’s most advanced chips. URL: https://www.computerhistory.org/siliconengine/moores-law-predicts-the-future-of-integrated-circuits/

M33 - Gordon E. Moore, “Cramming more components onto integrated circuits” (Electronics, April 19, 1965) - PRIMARY, via CHM classic-papers PDF

Read: SEARCH EXCERPTS of the article text (2026-11-01) Supports: minimum-cost logic - cost per component nearly inversely proportional to count, but yields fall with complexity, so a cost minimum exists and rises over time (then at 50 components per circuit, expected ~1,000 in five years); “The complexity for minimum component costs has increased at a rate of roughly a factor of two per year”; “by 1975, the number of components per integrated circuit for minimum cost will be 65,000”; two-mil component spacing; multilayer metallization anticipated; silicon expected to remain the basic material “because of the technology which has already evolved around it and its oxide, and because it is an abundant and relatively inexpensive starting material”; gallium arsenide foreseen for microwave functions. URL: https://www.computerhistory.org/semiconductor/assets/media/classic-papers-pdfs/Moore_1965_Article.pdf

P7 - R. H. Dennard, F. H. Gaensslen, H-N. Yu, V. L. Rideout, E. Bassous, A. R. LeBlanc, “Design of ion-implanted MOSFET’s with very small physical dimensions” (IEEE Journal of Solid-State Circuits, October 1974) - PRIMARY

Read: SEARCH EXCERPTS incl. scaling-transformation passage (2026-11-01) Supports: constant-field scaling transformation in three variables - all linear dimensions reduced by factor k (incl. oxide thickness and junction depth), applied voltages reduced by k, substrate doping increased by k; motivated by short-channel effects (threshold-voltage reduction from drain depletion penetration); worked example k=5 to 1-micron channel requiring ~200-angstrom gate insulator; fabricated polysilicon-gate MOSFETs with 0.5-micron channels; IBM authors. URL: https://doi.org/10.1109/jssc.1974.1050511

G1 - Wikipedia, “Dennard scaling” (secondary explainer)

Read: SEARCH EXCERPTS (2026-11-01) Supports: tabulated consequences of constant-field scaling - device area scales 1/k^2, intrinsic delay 1/k, power per device 1/k^2, power density constant; practical cadence: 0.7x linear shrink per generation doubles transistors per area, halves device power, raises frequency ~1.4x, keeps power density flat; contrast with fixed-voltage scaling (power density rises as k^3). Limitations: Wikipedia; used only to paraphrase the arithmetic consequences of the primary paper (P7), not for history or dates. URL: https://en.wikipedia.org/wiki/Dennard_scaling

G2 - Wikipedia, “Semiconductor device fabrication” (secondary compilation)

Read: SEARCH EXCERPTS (2026-11-01) Supports: process-node timeline (20 um 1968, 10 um 1971, 6 um 1974, 3 um 1977, 1.5 um 1981, 1 um 1984, 800 nm 1987, 600 nm 1990, 350 nm 1993, 250 nm 1996, 180 nm 1999, 130 nm 2001, 90 nm 2003, 65 nm 2005, 45 nm 2007, 32 nm 2009, 28 nm 2010, 22 nm 2012, 14 nm 2014, 10 nm 2016, 7 nm 2018, 5 nm 2020, 3 nm 2022, 2 nm 2025); node names decoupled from any physical gate length since the mid-1990s - marketing terms without standardized relation to feature size or density (Intel 10nm ~ TSMC 7nm density example); advanced-node fabrication takes 11-13 weeks on average, up to 15 weeks; wafer diameter timeline (25 mm 1960 to 300 mm by 2000); FOUP mini-environments; KLA’s first automatic reticle/mask inspection 1984 and wafer inspection 1985; Applied Materials Precision 5000 cluster tool. Limitations: Wikipedia; node-year table reflects common industry convention and matches ITRS records; used as timeline scaffolding, with node dates treated as approximate by +-1 year. URL: https://en.wikipedia.org/wiki/Semiconductor_manufacturing_processes

G3 - SIA, ITRS 2003 Overall Roadmap Technology Characteristics + 2013 Executive Summary (primary industry roadmap documents)

Read: SEARCH EXCERPTS (2026-11-01) Supports: the observed two-year technology-node cycle (350 nm/1995, 250 nm/1997, 180 nm/1999 as originally calculated; later DRAM-qualified data 1995/1998/2000/2002 with a one-year lag); DRAM interconnect half-pitch used as the representative node metric; consensus projection of a slowing three-year cycle in the 2003-2018 period and a “0.5x every 6 years” 3-year cycle anticipation in 2013; node-label “rounding” conventions corrected in 2003. URL: https://www.semiconductors.org/wp-content/uploads/2018/08/2003Overall-Roadmap-Technology-Characteristics.pdf

G4 - Bloomberg (via Yahoo Finance), “TSMC says ASML’s latest chipmaking gear is too pricey to use” (news, 2026-04-22)

Read: SEARCH EXCERPTS (2026-11-01) Supports: high-NA EUV machines fetch upwards of 350 million euro (~$410 million) apiece; TSMC has no current plans to adopt high-NA EUV for production through 2029; TSMC's A13 node planned for production in 2029; a state-of-the-art chip plant takes roughly $20-30 billion to build; ASML entry-level EUV machines cost more than $200 million; TSMC 2026 capital expenditure could approach $56 billion; ASML expects high-NA to enter high-volume production in 2027-2028. URL: https://www.bloomberg.com/news/articles/2026-04-22/tsmc-says-asml-s-latest-chipmaking-gear-is-too-pricey-to-use (reprint: https://sg.finance.yahoo.com/news/tsmc-says-asml-latest-chipmaking-183735725.html)

G5 - Simon-Kucher, "The end of automatic cost decline: Rethinking Moore's Law in the modern era" (consulting analysis)

Read: FULL (web page, 2026-11-01) Supports: single advanced-node fab now costs $15-20 billion; industry-wide semiconductor capex projected ~$160 billion for 2025; TSMC 2025 capex guidance $40-42 billion, roughly 70 percent to advanced process technologies; ASML current-generation EUV systems start ~$220 million per unit; High-NA EUV ~$380 million each; prospective Hyper-NA (early 2030s) could exceed $700 million per unit; leading-edge manufacturers fell from a dozen (2000) to six (2010) to three (2026); at 2nm, shrinking no longer lowers cost per transistor (TSMC 2nm wafer ~$30,000 vs 3nm ~$20,000); TSMC has committed $165+ billion to US fab investments. Limitations: consulting synthesis; figures are approximations consistent with G4 and G6. URL: https://www.simon-kucher.com/en/insights/end-automatic-cost-decline-rethinking-moores-law-modern-era

G6 - BCG, "Navigating the Costly Economics of Chip Making" (2023)

Read: SEARCH EXCERPTS (2026-11-01) Supports: 2026-era greenfield advanced-logic fab ten-year total cost of ownership $35-43 billion, 33-66% above 2023 costs; EUV tools ~twice the $150-million-plus price of earlier machines; high-NA EUV 0.55 NA vs 0.33 NA, 8nm vs 13nm resolution; complexity (more mask layers, more steps) as top cost driver. URL: https://www.bcg.com/publications/2023/navigating-the-semiconductor-manufacturing-costs

G7 - ASML corporate history pages (asml.com/en/company/about-asml/history and stories "Making EUV: from lab to fab", "ASML's founding story")

Read: SEARCH EXCERPTS (2026-11-01) Supports: ASM Lithography founded April 1, 1984 as Philips + ASM International JV to commercialize the Philips-developed PAS 2000 stepper; began in a leaky shed in Eindhoven with 47 of 50 offered Philips employees signing on; PAS 2500 (1986) with new alignment technology; Zeiss partnership established 1986; PAS 5500 breakthrough platform in the 1990s; IPO 1995 (Amsterdam and New York), Philips exiting over following years; TWINSCAN dual-stage 2001; first immersion machine TWINSCAN AT:1150i in 2003; first volume immersion XT:1700i 2006; XT:1900i NA 1.35 in 2007; EUV program started 1997 (Jos Benschop); European EUCLIDES consortium 1998 with ZEISS and Oxford Instruments; joined US EUV LLC in 1999; EUV wavelength settled at 13.5 nm from tin plasma; LPP source hits tin droplets 50,000 times per second twice, plasma ~40x hotter than sun's surface; first pre-production NXE:3100 shipped 2010 to a Samsung research facility; Cymer acquired 2013; NXE:3300 first production system 2013, NXE:3350 in 2015, production-ready NXE:3400 ordered in batches from 2016; 2012 Customer Co-Investment Program with Intel, Samsung, TSMC; 250 W source enabling 125 wafers/hour; first EUV-enabled commercial product Samsung Galaxy Note10 in 2019; 100th EUV system December 2020; 127 latest-gen EUV machines in use by end of 2021; Benschop's admission EUV was 13 years late vs the naive 2006 forecast. Limitations: company history, celebratory framing; dates and specs corroborated across ASML and independent coverage. URL: https://www.asml.com/en/company/about-asml/history ; https://www.asml.com/en/company/stories/2022/making-euv-lab-to-fab ; https://www.asml.com/en/company/stories/2024/asml-founding-story

G8 - Wikipedia, "ASML" (secondary)

Read: SEARCH EXCERPTS (2026-11-01) Supports: ASML became world's largest lithography supplier by 2002; Intel invested $4.1 billion in ASML in July 2012 for a 15% stake under the co-investment program, Samsung and TSMC taking smaller stakes; ASML's EUV LLC membership carried commitments including a US research center and sourcing 55% of components for US-sold machines from US suppliers; Cymer acquisition announced October 2012 for $2.55 billion, completed May 2013; IMEC produced first functional 22nm SRAM cells with prototype EUV in 2009; production EUV shipping from 2018; Dutch and US export controls on ASML sales to China. URL: https://en.wikipedia.org/wiki/ASML

G9 - CINNO IC Research 2024 top-10 equipment ranking (via futunn/EET-China) + Gartner WFE 2024 summary

Read: SEARCH EXCERPTS (2026-11-01) Supports: 2024 wafer-fab-equipment market ~$111.6 billion, up 8.6% (Gartner); top five unchanged: ASML (>$30 billion semiconductor-equipment revenue), Applied Materials (~$25 billion, "supermarket" spanning deposition, implant, etch, CMP, inspection), Lam Research (etch/deposition/clean); top five collectively ~$90 billion, about 85% of top-10 revenue; NAURA the sole Chinese firm in top 10, up to sixth. Limitations: third-party analyst estimates; revenue conversions at stated exchange rates. URL: https://news.futunn.com/en/post/53871605/ ; https://www.gartner.com/en/documents/6430207

N1 - Computer History Museum, "Analog Integrated Circuits" (Revolution exhibit)

Read: SEARCH EXCERPTS (2026-11-01) Supports: analog ICs convert continuously varying signals (sound, light, heat) for digital processing; analog ICs enjoy far longer useful lives than digital - many basic functions still useful after 40+ years; Robert Widlar with process engineer Dave Talbert kick-started the

analog IC business at Fairchild and National; Widlar legends (the axe, the sheep for National's lawns); uA741 by David Fullagar, 1968, most popular op-amp of all time. URL: https://www.computerhistory.org/revolution/digital-logic/12/281

N2 - CHM, "Operational Amplifier Milestones" (from Kent Lundberg's Op Amp History lecture)

Read: SEARCH EXCERPTS (2026-11-01) Supports: feedback-amplifier lineage - Nyquist 1932 stability criterion, Black's 1934 "Stabilized Feedback Amplifiers", Bode 1940; term "operational amplifier" coined by John Ragazzini 1947; Philbrick K2-W tube op amp 1952 (~$22); first transistorized (germanium) op amps 1958; first silicon op amps 1960; TI Series 52 linear IC family 1962; NASA IMP satellite first spacecraft with ICs 1963; Zenith hearing aid first commercial analog-IC product 1964; Fairchild uA702 first IC op amp 1964 (Widlar); uA709 1965 "first IC op amp that works like an op amp"; Widlar's LM101 at National 1967; Fullagar's internally compensated uA741 1968; LM101A/LM107 1968; LF156 JFET-input 1974; OP-07 precision 1975. URL: https://archive.computerhistory.org/resources/access/text/2017/03/102770853-05-01-acc.pdf

N3 - IEEE Spectrum, "Chip Hall of Fame: Fairchild uA741 Op-Amp"

Read: SEARCH EXCERPTS (2026-11-01) Supports: uA702 sold at $300 each; uA709 cut cost to $70 and was a huge commercial success; Widlar quit over a raise and joined National, creating the LM101 (1967), a version still in production; Fullagar found the LM101 front end overly sensitive to noise from semiconductor quality variation; his fix - a couple of extra transistors - came to him driving to Tahoe; Gordon Moore, then head of R&D, routed the design to production; the 741 and competitor variants have sold in the billions and remain in production; for the 702's $300 price you can buy ~1,700 modern 741s. URL: https://spectrum.ieee.org/chip-hall-of-fame-fairchild-semiconductor-a741-opamp

N4 - Intel, "A Success...Out of Quality Control Issues" (virtual vault, EPROM history)

Read: SEARCH EXCERPTS (2026-11-01) Supports: 1969 Intel reliability problems with the 1101 SRAM (first mass-produced MOS chip); Dov Frohman found silicon-dioxide insulators absorbing electrons and holding charge; he turned the defect into the EPROM - electrically programmable, nonvolatile, erasable by UV through a quartz window; prototype debuted February 1971 at ISSCC Philadelphia; Moore's account of the UV-erasure demo ending on the Intel logo and audience applause; EPROM cut chip prototype design time from days/weeks to hours; EPROM and the microprocessor grew together; Intel's EPROM business grew into the 1980s. URL: https://www.intel.com/content/www/us/en/history/virtual-vault/articles/eprom.html

N5 - CHM blog, "Pioneers of Semiconductor Non-Volatile Memory (NVM): The First Four Decades" + Masuoka oral history (2012)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Frohman-Bentchkowsky joined Fairchild R&D 1965, PhD on MNOS charge trapping; at Intel from 1969 conceived the FAMOS floating-gate device; unaware of Kahng/Sze Bell Labs floating-gate work until his patent filing; Intel 1702, a 2048-bit EPROM, introduced 1971; cheaper one-time-programmable windowless versions popular with microprocessor systems; EPROMs Intel's most profitable line until the mid-1980s; 1980 Masuoka at Toshiba's Kawasaki R&D center recruited Asano, Iwahashi, Komuro, Tanaka for a single-transistor-cell NVM; colleague Shoji Ariizumi suggested the name "flash" (erasure as fast as a camera flash); NOR flash described at IEDM 1984 but Toshiba did not pursue it commercially (triple-poly manufacturing issues); Exel's Mukherjee/Chang manufacturable design became the basis of Intel's NOR flash; Masuoka conceived NAND flash while in Washington DC on TI patent litigation; 1987 IEDM NAND paper; 16-Mbit NAND flash production began 1992; Masuoka's earlier double-gate EPROM (1973) programmed in ~100 microseconds vs Intel's milliseconds, same UV erase. URL: https://computerhistory.org/blog/pioneers-of-semiconductor-non-volatile-memory-nvm-the-first-four-decades/ ; https://archive.computerhistory.org/resources/access/text/2013/01/102746492-05-01-acc.pdf

N6 - B. Jayant Baliga, "Creation of the Insulated Gate Bipolar Transistor" (Wiley book chapter, DOI 10.1002/9781394202478.ch25)

Read: SEARCH EXCERPTS (2026-11-01) Supports: IGBT conceived at GE - Baliga's patent disclosure July 26, 1977 for an MOS-gate thyristor structure; first experimental IGBT-mode measurements July 30, 1979 (V-MOS structure, lead process technician Margaret Lazeri); published September 27, 1979 in Electronics Letters; first production-line IGBT wafers August 1981 with 600 V blocking and ~1 V on-state drop at 100-200 A/cm2; GE released the first IGBT product June 20, 1983 (D94FQ4,R4, 400/500 V, 18 A), 2-3 years before any Japanese product; Baliga rebuts the "IGBT born in Japan 1985" claim. Limitations: inventor's own account; used for GE timeline, with the Japan-priority dispute noted and avoided in prose. URL: https://doi.org/10.1002/9781394202478.ch25

N7 - Electronic Design, "Advances in Discrete Semiconductors March On"

Read: SEARCH EXCERPTS (2026-11-01) Supports: power-MOSFET lineage - Hitachi VMOS ~1969, Siliconix VMOS 1975, International Rectifier HEXFET 1978; Nathan Zommer built the first IGBTs under Baliga's direction at Intersil's Cupertino line (January 1981 meeting) and later founded IXYS (1983); IGBT = MOSFET gate + bipolar conduction, low conduction losses at high voltage; modern IGBTs switch in under 100 ns vs 3 microseconds twenty years earlier. URL: https://www.electronicdesign.com/content/article/21188363/advances-in-discrete-semiconductors-march-on

N8 - GE News, “Standing On Edison’s Shoulders” (Holonyak LED retrospective) + MRS Bulletin, “How Holonyak won the race to invent visible LEDs”

Read: SEARCH EXCERPTS (2026-11-01) Supports: Nick Holonyak Jr., Bardeen’s first PhD student (1954), joined GE Syracuse after Bell Labs (under John Moll) and the Army; pursued III-V direct-gap alloys (GaAsP) against colleagues’ doubts; Robert Hall at GE Schenectady demonstrated the first semiconductor laser (GaAs, infrared, reported September 1962, published November 1, 1962 in PRL) with near-simultaneous GaAs laser reports from IBM (Nathan) and MIT Lincoln Lab (Quist); Holonyak demonstrated the first visible semiconductor laser/LED (red, GaAsP) on October 9, 1962 - “the first visible semiconductor laser and LED”; Holonyak conceded Hall “got there ahead of me” but is credited as inventor of the LED. URL: https://www.ge.com/news/reports/standing-on-edisons-shoulders-fifty-years-ago ; https://www.cambridge.org/core/journals/mrs-bulletin/article/50-years-ago-how-holonyak-won-the-race-to-invent-visible-leds/8A20CA7B75C337853C5328449851A663

N9 - ETHW Milestones, “First Practical Photovoltaic Solar Cell” (IEEE)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Bell Labs’ Chapin, Fuller, Pearson demonstrated the first practical silicon solar cell April 25, 1954 at ~6% efficiency; origin in Pearson/Fuller’s accidental observation of photocurrent in a lithium-treated gallium-doped silicon sample; Chapin’s 2.3% measurement of Pearson’s sample; Fuller’s arsenic/boron diffused structure with anti-reflection coating reaching ~6%; public demo powered a 21-inch Ferris wheel; 50 watts per square yard vs RCA’s strontium-90 “atomic battery” at a millionth of a watt; powered Vanguard 1 (March 1958) and virtually all satellites since; Telstar’s power source. URL: https://ethw.org/Milestones:First_Practical_Photovoltaic_Solar_Cell

B1 - TSMC corporate “About TSMC” + Wikipedia “TSMC” + Nature Electronics “Taiwan and the global electronics industry” + CHM Morris Chang/Jen-Hsun Huang conversation (2007)

Read: SEARCH EXCERPTS (2026-11-01) Supports: TSMC established 1987 by Morris Chang as the world’s first dedicated/pure-play foundry; 2025 stats: 12,682 products, 305 technologies, 534 customers, >17 million 12-inch-equivalent wafers annual capacity, six 12-inch GIGAFABs in Taiwan plus subsidiaries in Nanjing, Arizona, JASM Japan, Washington, China, Dresden fab construction began 2024 (28/22nm planar, 16/12nm FinFET); founding capital structure - Taiwan government National Development Fund 48.3%, Philips 27.6% ($58M plus technology transfer and IP licensing), ~20% from eight Taiwanese private companies “asked” by the government, 4.1% KMT investment arm; TI and Intel declined to invest; first CEO James E. Dykes (ex-Philips) left after a year, Chang became CEO; total initial investment $220 million; 1997 NYSE listing at ~$6 billion market cap; ~43% CAGR over first 20 years (to ~$10B revenue, ~$60B market cap in 2007, second only to Intel); Chang’s three founding values (integrity, commitment, innovation); Li Kwoh-ting invited Chang to head ITRI in 1985/86 with “a blank cheque” to build Taiwan’s chip industry; 1970s government strategy: technology transfer from the US, research institutes, spin-offs. Limitations: Wikipedia for the capital structure detail; corroborated by Nature Electronics and the NTU SPSR center page. URL: https://www.tsmc.com/english/aboutTSMC ; https://en.wikipedia.org/wiki/TSMC ; https://www.nature.com/articles/s41928-021-00581-1 ; https://archive.computerhistory.org/resources/access/text/2012/05/102658254-05-01-acc.pdf

B2 - WSTS fall 2024 forecast + PwC “State of the semiconductor industry” + McKinsey “Silicon squeeze: AI’s uneven impact”

Read: SEARCH EXCERPTS (2026-11-01) Supports: 2024 global semiconductor market ~$627 billion, +19.0% YoY (WSTS), memory +81%, logic +16.9%; 2025 forecast ~$697 billion (+11.2%); global chip shortage from H2 2020 through end of 2022 (pandemic demand surge), then oversupply and a 2023 downturn; projected path to ~$1 trillion by 2030 (PwC/Omdia series: 2020 $476B, 2021 $595B, 2022 $598B, 2023 $544B, 2024 $642B); McKinsey economic-profit analysis: $38B aggregate 2000-09 (mostly Intel), $450B 2010-19, $473B 2020-24; AI-linked segment CAGR 21% 2019-2023 vs 6% overall; middle 90% of companies’ per-company economic profit fell from $130M (2021 average) to $17M by 2024; BEVs carry more than double the semiconductor content of ICE cars; semiconductor content per vehicle $420 (2019) to ~$800 (2023). URL: https://www.wsts.org/esraCMS/extension/media/f/WST/6765/WSTS_FC-Release-2024_11.pdf ; https://www.pwc.com/gx/en/industries/technology/state-of-the-semiconductor-industry-report.pdf ; https://www.mckinsey.com/industries/semiconductors/our-insights/silicon-squeeze-ais-impact-on-the-semiconductor-industry

B3 - Gordon Moore, “Lithography and the Future of Moore’s Law” (1995 SPIE speech, Auburn-hosted PDF)

Read: SEARCH EXCERPTS (2026-11-01) Supports (PRIMARY - Moore’s own words): original 1965 plot doubled complexity every year up to 1965, extrapolated a decade to 64,000-component circuits by 1975; 1975 IEDM update changed slope to doubling every two years with a five-year rollover; equipment cost ~$12,000 per tool when Intel founded its fab in 1968, heading to $12 million by the late 1990s, without proportional throughput gains; billion-dollar fabs already passed, $2-3 billion plants by 1998; “capital costs are rising far faster than revenue in the industry”; little room left in manufacturing efficiency; Moore declined to extrapolate beyond 0.18 micron - “terra incognita.” URL: https://eng.auburn.edu/~agrawvd/COURSE/E7770_Spr07/READ/1995_SPIE_Speech.pdf

B4 - Semiconductor Engineering, “Piecing Together Chiplets” and “Making Chips At 3nm And Beyond” (IBS/Handel Jones design-cost figures)

Read: SEARCH EXCERPTS (2026-11-01) Supports: average chip design cost ~$40M at 28nm, ~$217-222M at 7nm, ~$416-436M at 5nm, ~$590-650M at 3nm (IBS); Sarasin: foundries signaled slowing cost declines from ~2011; lithography cost rises exponentially below 28nm; AMD and Nvidia reported increased costs and skipped a node. Limitations: analyst estimates via trade press; two SemiEngineering pieces differ slightly (7nm $217M vs $222.3M, 5nm $416M vs $436.3M, 3nm $590M vs $650M) - prose uses rounded ranges. URL: https://semiengineering.com/piecing-together-chiplets/ ; https://semiengineering.com/making-chips-at-3nm-and-beyond/ ; https://sarasinandpartners.com/row/think/theres-life-in-the-old-law-yet/

B5 - Wikipedia, “Rock’s law” (Moore’s second law)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Rock’s law / Moore’s second law - cost of a fab doubles roughly every four years, reaching ~$14 billion as of 2015; framed as the economic flip side of Moore’s law; some argue fab costs plateaued in the late 1990s and cost per transistor is the more relevant constraint. URL: https://en.wikipedia.org/wiki/Rock%27s_law

B6 - US Bureau of Industry and Security: October 7, 2022 interim final rule and October 17, 2023 updates (BIS press pages + Federal Register 2023-23055)

Read: SEARCH EXCERPTS (2026-11-01) Supports (PRIMARY government documents): October 7, 2022 BIS interim final rule established new controls on advanced computing ICs, computer commodities containing them, supercomputer end uses, certain semiconductor manufacturing equipment, end-use controls on development/production of three types of advanced-node ICs, and restrictions on “U.S. person” activities; stated purpose - restricting the PRC’s ability to obtain critical technologies for military modernization; October 17, 2023 updates (effective November 2023) replaced the interconnect-bandwidth parameter with a performance-density threshold, created the Notified Advanced Computing license exception, expanded licensing to 21-22 arms-embargoed countries plus Macau, added worldwide licensing for firms headquartered in those destinations, imposed controls on additional equipment types, and codified foundry due-diligence red flags. URL: https://www.bis.gov/press-release/commerce-strengthens-restrictions-advanced-computing-semiconductors-semiconductor-manufacturing-equipment ; https://www.federalregister.gov/documents/2023/10/25/2023-23055/implementation-of-additional-export-controls-certain-advanced-computing-items-supercomputer-and

B7 - US CHIPS and Science Act: CRS report R49031 + AIP FYI coverage (primary/near-primary)

Read: SEARCH EXCERPTS (2026-11-01) Supports: CHIPS and Science Act (P.L. 117-167, Division A) signed August 9, 2022; ~$52 billion total - $39 billion manufacturing incentives through FY2026, $11 billion Commerce R&D programs, $2 billion DoD microelectronics network; up to $6 billion of the $39B as loans/guarantees; 25% investment tax credit (CBO estimate ~$24 billion through 2031); final commercial-fab awards: Intel $7.86B (Nov 26, 2024) plus ~$3B DoD Secure Enclave with the US taking equity (~$8.9-9.9B total direct), TSMC Arizona $6.6B final award Nov 15, 2024 (total incentives listed $11.565B) supporting a $65B three-fab Phoenix investment, Samsung $4.745B, Micron $6.165B, GlobalFoundries $1.587B, TI $1.61B, SK hynix $958M; Intel Ohio initial $20B commitment with talk of $100B expansion; Micron $40B through 2030. URL: https://www.congress.gov/crs-product/R49031 ; https://www.aip.org/fyi/huge-chips-grants-awarded-to-tsmc-samsung-and-micron ; https://www.aip.org/fyi/2022/chips-act-funding-sets-semiconductor-initiatives-motion

B8 - Taiwan’s chip dominance: Reuters special report (Dec 27, 2021) + Economist special report (Mar 2023) + Guardian (Jul 2024)

Read: SEARCH EXCERPTS (2026-11-01) Supports: TSMC accounts for more than 90% of global output of the most advanced semiconductors (industry estimates); Taiwan produces over 60% of the world’s semiconductors overall; chips ~15% of Taiwan’s GDP; “silicon shield” framing - Taiwan made itself indispensable to both superpowers; Chris Miller: only three companies produce anything close to the cutting edge (Intel, Samsung, TSMC). URL: https://www.reuters.com/article/technology/special-report-taiwan-chip-industry-emerges-as-battlefront-in-us-china-showdow-idUSL4N2TC0JE/ ; https://www.economist.com/special-report/2023/03/06/taiwans-dominance-of-the-chip-industry-makes-it-more-important ; https://www.theguardian.com/world/article/2024/jul/19/taiwan-semiconductor-industry-booming

B9 - Chip Supply Chain project (chipsupplychain.org) chemicals/gases/photoresist brief + OECD “Mapping the semiconductor value chain” (2025) + SemiconductorX Bottleneck Atlas

Read: SEARCH EXCERPTS (2026-11-01) Supports: Japanese firms held 78% of world photoresist sales in 2023 (Fuji Keizai); five Japanese resist makers (JSR, Tokyo Ohka Kogyo, Shin-Etsu, Fujifilm, Sumitomo); resist qualification takes 7-17 months (SIA 2023); pre-invasion Ukraine supplied ~70% of world neon and ~90% of US semiconductor-grade neon; Cryoin (Odesa) and Ingas (Mariupol) shut in 2022; neon fills lithography lasers (not EUV, which uses tin); Shin-Etsu and SUMCO supply more than half the global silicon wafer market (OECD), with Shin-Etsu ~22% and SUMCO ~20% of global 300mm capacity (Eswin prospectus, end-2024); JSR taken private by Japan Investment Corporation 2024; atlas shares: EUV resist ~95% Japan; ABF film >95% Ajinomoto; EUV mask blanks entirely AGC/Hoya; gallium ~99% Chinese refining; rare-earth refining 91% China; high-purity quartz ~80% from Spruce Pine NC (Sibelco/The Quartz Corp); EDA - Synopsys ~$7.1B and Cadence ~$5.3B vs ~$185M for China’s largest; KLA ~74% of $12.9B inspection/metrology; Advantest ~65% of $9.0B test; TSMC 72.5% of foundry revenue (2Q26) with 79% of its wafer revenue at 7nm and finer; HBM shares SK hynix 50/Samsung 33/Micron 18 (2Q26); CoWoS assembly entirely in Taiwan; ASE 44.6% of top-10 OSAT revenue (2024); BESI leads hybrid bonding. Limitations: atlas figures are compiled estimates from cited primary reports; market shares are point-in-time (2024-2026). URL: https://chipsupplychain.org/pdf/chemicals-gases-and-photoresist.pdf ; https://www.oecd.org/content/dam/oecd/en/publications/reports/2025/06/mapping-the-semiconductor-value-chain_5ba52971/4154cdbf-en.pdf ; https://semiconductorx.com/semiconductor-bottleneck-atlas.html

B10 - Kleinhans & Hess, “Understanding the Global Chip Shortages” (SNV, Nov 2021) + Korea Times shortage coverage

Read: SEARCH EXCERPTS (2026-11-01) Supports: February 2021 Texas winter storm forced weeks-long shutdowns at Samsung, NXP, Infineon Austin fabs with hundreds of millions in losses; chip designs are locked to a specific foundry’s process node, so production cannot simply move; three-month average fab cycle means shocks translate directly into lost output and rising lead times; 2021 Japan earthquake hit Renesas and Shin-Etsu; March 2021 fire at Renesas Naka (Hitachinaka) fab; Unimicron PCB plant fire February 2021. URL: https://jpkleinhans.de/worklog_topics/2021-11_SNV_Understanding_the_Global_Chip_Shortages_Kleinhans_Hess.pdf ; https://www.koreatimes.co.kr/business/tech-science/20210323/industries-grappling-with-deepening-chip-shortage

F1 - FinFET/GAA primary materials: UC Berkeley research news (2011) + MIT Technology Review (May 6, 2011) + Intel Tri-Gate press release (May 2011) + Intel process/packaging roadmap release (2021) + Samsung GAA press release (June 30, 2022)

Read: SEARCH EXCERPTS (2026-11-01) Supports: FinFET invented at UC Berkeley - Chenming Hu wrote the specs on a 1996 flight to Japan; Hu, Jeffrey Bokor, Tsu-Jae King Liu built and named the FinFET in 1999, under a DARPA challenge to scale below 25nm; Berkeley released the IP into the public domain; by 2002 ITRS favored FinFET and SOI for the next 15 years; Intel Tri-Gate announced May 4, 2011 as “the most radical shift in semiconductor technology in 50 years,” in high-volume 22nm production (Ivy Bridge) by end of 2011, up to 37% faster at low voltage or under half the power vs 32nm planar; Intel’s transitions: strained silicon at 90nm, high-k metal gate at 45nm, FinFET at 22nm; Intel 20A (RibbonFET GAA + PowerVia backside power, “angstrom era”) planned to ramp 2024, 18A for early 2025, first high-NA EUV tool expected; Samsung began initial 3nm GAA (MBCFET nanosheet) production June 30, 2022 - first nanosheet in production - claiming up to 45% lower power, 23% higher performance, 16% smaller area vs 5nm. Limitations: company press claims for performance percentages; dates and architecture facts corroborated by independent coverage. URL: https://vcresearch.berkeley.edu/news/radical-new-intel-transistor-based-uc-berkeleys-finfet ; https://www.technologyreview.com/2011/05/06/194868/how-three-dimensional-transistors-went-from-lab-to-fab/ ; https://www.intc.com/news-events/press-releases/detail/655/intel-reinvents-transistors-using-new-3-d-structure ; https://www.intc.com/news-events/press-releases/detail/1486/intel-accelerates-process-and-packaging-innovations ; https://news.samsungsemiconductor.com/global/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture/

F2 - Nikonov & Young et al., “Beyond CMOS computing with spin and polarization” + IRDS 2024 Beyond CMOS chapter + APL Materials low-power roadmap

Read: SEARCH EXCERPTS (2026-11-01) Supports: “Boltzmann tyranny” - thermal distribution limits any barrier-switched charge device to at best 60 mV/decade current modulation, keeping high-performance CMOS supply voltage above ~0.5 V; TFETs can beat 60 mV/decade via tunneling; new state variables (spin, polarization, strain, photon intensity) as a path beyond CMOS; collective-switch framework for spintronic/multiferroic logic; practical-switching energy floor ~100 kBT (about 50x below aggressively scaled CMOS at ~10^4 kBT); Landauer limit kBT ln 2 for irreversible logic, approached only asymptotically; error rates in digital logic kept below 10^-14; neuromorphic/in-memory architectures and approximate/stochastic computing as complexity-scaling paths; FeFET and 2D-materials devices on the IRDS beyond-CMOS roadmap. URL: https://knowen-production.s3.amazonaws.com/uploads/attachment/file/3731/Beyond%2BCMOS%2Bcomputing%2Bwith%2Bspin%2Band%2Bpolarization.pdf ; https://irds.ieee.org/images/files/pdf/2024/2024IRDS%5FBC.pdf

E1 - IEA “Electricity 2024” and “Energy and AI” (2025) + Reuters on Taiwan’s chip power demand (2024)

Read: SEARCH EXCERPTS (2026-11-01) Supports: data centres consumed ~415 TWh (~1.5% of world electricity) in 2024; US 45%, China 25%, Europe 15% of that; ~12% annual growth since 2017, ~15% per year 2024-2030; IEA base case projects over 1,000 TWh by 2030 and ~1,300 TWh by 2035; earlier 2024 report projected possible doubling to >1,000 TWh by 2026; data-centre electricity CO2 emissions peaking ~320 Mt by 2030 in base case, still <1% of global CO2; TSMC alone consumed 6.4% of Taiwan’s electricity in 2021; Taiwan makes ~60% of the world’s chips with a highly energy-intensive process. URL: https://www.iea.org/reports/electricity-2024/executive-summary ; https://www.iea.org/reports/energy-and-ai/executive-summary ; https://www.iea.org/reports/energy-and-ai/energy-supply-for-ai ; https://www.reuters.com/sustainability/climate-energy/how-taiwans-green-power-deficit-threatens-tech-industrys-bid-net-zero-2024-06-04/

I8 / S1 - Sony Group official corporate history, Chapter 3 “Developing the Transistor Radio” (sony.com)

Read: FULL TEXT (2026-11-01) Supports: license fee $25,000 (nine million yen); Ibuka learned of WE licensing on his March-May 1952 US trip; MITI initially refused (“too advanced for a shabby weed-covered factory”); Morita provisionally signed the WE contract August 1953 contingent on MITI approval, which then followed; Regency TR-1 credited by Sony itself as the world’s first transistor radio (announced late 1954, Christmas-season sales); TR-52 prototype completed January 1955, first article to carry the SONY logo, scrapped after its grille warped in May heat; TR-55 - Japan’s first transistor radio - on sale September 1955 per Sony’s official history (many secondary sources say August; Sony’s own page preferred for this Sony-specific claim); the “first fully in-house radio” claim is Sony self-description, to be quoted with attribution only; TR-63 “Pocketable” 1957 at $39.95 US; company renamed Sony January 1958. Additional detail: Yamada built the Western Electric relationship in New York; WE impressed by Totsuko’s unaided tape-recorder development. CONFLICT NOTED: TR-55 market timing - Sony’s own narrative says September 1955; the academic paper (I9) records the TR-55 shown July 23, 1955 with sales starting the following month (August), and Wikipedia agrees with August. Use “summer 1955” or “shown in July, on sale within weeks” in prose. Note:

registered twice under [I8] and [S1]; merged. [I8] citations resolve here. URL: https://www.sony.com/en/SonyInfo/CorporateInfo/History/SonyHistory/1-03.html

S2 - TSMC Q3 2026 earnings call transcript and 3Q26 Management Report (investor.tsmc.com, 2026-10-15) + Forbes/Tom's Hardware ramp coverage

Read: SEARCH EXCERPTS (verbatim, substantial, 2026-11-01) Supports: N2 contributed 8% of wafer revenue in Q3 2026 (N3 33%, N5 28%, N7 10%; 7nm-and-below 79% of wafer revenue); gross margin 66.4%, down 1.3pp sequentially "primarily due to margin dilution from 2-nanometer ramp" (CFO Wendell Huang); Q3 revenue $46.72B; high-volume N2 manufacturing began Q4 2025, ramping at Fab 20 (Hsinchu) and Fab 22 (Kaohsiung), targeting five facilities within the first year. URL: https://investor.tsmc.com/chinese/encrypt/files/encrypt_file/reports/2026-10/eba4fac72873bf546b669bd2b5d973df5c93215d/TSMC%203Q26%20Transcript.pdf

S3 - Intel Q3 2026 results press release (2026-10-29) + Post-Hype Tech yield-claims verification (2026-10-31)

Read: FULL TEXT (2026-11-01) Supports: 18A in volume production for Intel's own products by late 2026; yield claims only on the earnings call, not in the release - CFO Zinsner: "Intel 18A yields continued their upward trajectory to industry standard levels" (no figure); CEO Tan: yields increasing "at a double-digit rate"; 18A costs down ~40% since Q1 2026; 18A-based chips from under 5% to nearly a third of Intel client CPU revenue; Intel Foundry Q3 revenue $6.7B (+58% YoY), operating loss $1.85B; external-customer revenue $411M (~6%), mostly one programme; no external 18A customer named ("will not disclose customer details"); 14A 0.9 PDK released October 2026; ASML High-NA readiness collaboration; RAMP-C completed. Limitations: yield and cost claims are Intel's own, unaudited; no external-customer confirmation. URL: https://www.intc.com/news-events/press-releases/detail/1786/intel-reports-third-quarter-2026-financial-results

S4 - Samsung SF2 status: Sammy Fans citing Chosun (2026-09-28) + Sekin analysis (2026-09-29)

Read: SEARCH EXCERPTS (2026-11-01) Supports: Exynos 2600 (Samsung's first 2nm GAA, SF2) ships in select Galaxy S26/S26+ units in the UK and other documented markets (US models use Snapdragon); first-gen SF2 yield "approaching 60%" per a Chosun industry report; reported SF2P improvements +12% performance / -25% power / -8% area. Limitations: ALL numbers press-reported; Samsung discloses no auditable yield figures. Prose attributes yields to the trade press explicitly. URL: https://www.sammyfans.com/2026/09/28/samsung-2nm-chip-process-making-some-serious-progress/ ; https://sekin.in/exynos-2600-powers-some-galaxy-s26-phones-but-did-samsung-fix-its-yield-problems/

S6 - IEEE Spectrum transistor-production estimates (Apr 2015; Nov 2022) + SIA 60th-birthday release (Dec 2007)

Read: SEARCH EXCERPTS (2026-11-01) Supports: ~2.5x10^20 transistors made in 2014 (8 trillion per second average); TechInsights forecast ~10^21 transistors for 2022 - "more transistors than were cumulatively made in all the years prior to 2017"; 6x10^18 produced in 2007; cumulative estimates 2.9x10^21 through 2014 and 1.3x10^22 through 2018 (Wikipedia tabulation); no credible 2026 annual figure exists - the honest statement is ~10^21 per year by the early 2020s with the date attached. URL: https://spectrum.ieee.org/transistor-production-has-reached-astronomical-scales ; https://spectrum.ieee.org/transistor-density

S7 - Bell 1952 licensing terms (cross-reference entry)

Cross-reference, not a separate source. The licensing-terms facts cited as [S7] in the text are registered with their sources at [P2] (royalty structure, the $25,000 advance, the 1953 reduction to 2%, the hearing-aid waiver, diffusion effects) and at [H18] and [H19] (the 1951-1952 symposia and licensing history).

S8 - Hearing-aid economics and CK722 price curve: CHM Silicon Engine consumer-products page + IEEE Spectrum "The Irresistible Transistor" (2003) + Wikipedia CK722 (citing Ward/IEEE) + PBS hearing-aid page

Read: SEARCH EXCERPTS (2026-11-01) Supports: CK703 point-contact in production 1948 but too unstable; CK718 alloy junction released in volume (10,000 units) end of 1952, assembled in repurposed infant incubators; hearing-aid rejects relabeled CK721/CK722; CK722 introduced early 1953 at $7.60, $3.50 by late 1954, $0.99 by 1956; Sonotone hybrid hearing aid December 1952 at $229.50 (two subminiature tubes + one Germanium Products transistor); Maico all-transistor aid 1953; 97% of hearing aids fully transistorized by 1954; Raytheon the world's largest transistor manufacturer 1952-1955 on hearing-aid volume (Norman Krim); Acousticon single-transistor design at $74.50; user battery costs fell from ~$100 to ~$10 per year; 1954 germanium transistors $10-15 a piece, TI drove TR-1 transistor cost to ~$2.50, Haggerty committed $2M (~10% of TI revenue). URL: https://www.computerhistory.org/siliconengine/transistorized-consumer-products-appear/ ; https://spectrum.ieee.org/the-irresistible-transistor ; https://en.wikipedia.org/wiki/CK722 ; https://www.pbs.org/transistor/background1/events/hearingaid.html

I11 - Semiconductor Industry History Society of Japan (SHMJ), "80s Trends in the Semiconductor Industry" (shmj.or.jp)

Read: FULL (web page, 2026-11-01) Supports: Japanese manufacturers held about 25% of the world semiconductor market in 1980, the US more than half; Japanese DRAMs acclaimed by US computer makers for quality, delivery and price; Japanese 64K-DRAM share overtook the US in 1981; overall Japanese DRAM share reached 80% in 1987, mainly on 256K parts; US manufacturers withdrew from the DRAM business; June 1985 SIA section-301 dumping complaint plus Micron (64K DRAM) and Intel (EPROM) suits, with a 1986 ITC injury ruling on 64K DRAMs; September 1986 US-Japan Semiconductor Trade Agreement (foreign market access, dumping prevention, suspension of US anti-dumping inquests); Europe's 1984 EUREKA program ($5.8 billion) and the founding of IMEC. URL: https://www.shmj.or.jp/english/trends/trd80s.html

I12 - Samsung's 1983 entry and DRAM climb: Samsung Global Newsroom corporate history + Korea Heritage Service registry entry + Asia Business Daily 40th-anniversary account + Nikkei xtech DRAM column

Read: FULL (Samsung page, 2026-11-01) / SEARCH RESULTS (heritage registry, Asia Business Daily, Nikkei, 2026-11-01) Supports: founding chairman Lee Byung-chul's "Tokyo Declaration" of February 8, 1983 announcing Samsung's entry into the semiconductor (DRAM) business; Samsung's 64K DRAM developed in 1983, the third in the world and first in Korea (Korea registered cultural heritage); Samsung introduced a 256K DRAM three months after its 64K and began mass production about seven months later, with US-subsidiary production from July 1985; Korean makers overtook Japan in DRAM in the late 1990s (Nikkei). URLs: https://news.samsung.com/global/history-of-samsung-7-semiconductor-breakthroughs-and-high-profile-sponsoring-1984-1985 ; https://www.asiae.co.kr/en/article/2023020616402970806 ; https://xtech.nikkei.com/dm/article/COLUMN/20131225/324816/ ; https://digital.khs.go.kr/heri/heriDetail.do?ctptNo=4413105630000&ctptUid=13983497628767031144